COMPUTER PERIPHERALS®

KEY TO LOGIC SYMBOLOGY

FOR LINE PRINTER EQUIPMENT

Computer Peripherals Inc
Printer Products Div

CUSTOMER ENGINEERING MANUAL

COMPUTER PERIPHERALS®

KEY TO LOGIC SYMBOLOGY

FOR LINE PRINTER EQUIPMENT

95390100

REVISION RECORD

REVISION	DESCRIPTION
A 9-75	Initial issue of the key to logic symbology for all line printers
B 4-76	Updated by incorporating sheets 88 thru 126.
C 5-76	Update by incorporating sheets 115 thru 122.
D 6-76	Updated by incorporating sheets 127, 128, 129, & revised sheet 84.
E 9-76	Updated by incorporating sheets 130 thru 146 & Revised sheets 64 & 78.
F 8-77	Updated by incorporating sheets 2A, 2B, 101 and 147 thru 153.
G 1-78	Updated by incorporating, the following change sheet 12 and adding sheets 154 thru 169.
H 7-78	Updated by incorporating the following: Change sheets 2A, 2B, and including sheets 154 thru 169.
I 4-79	Updated by incorporating the following : Change sheets 90, 154, 155 and 156.

PUBLICATION NO.
95390100

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140	7400	3		NAND GATE
141	7410	4		NAND GATE
146	7404	5		INVERTER
146L	74L04	6		INVERTER
1469	74S04	7		INVERTER
148	7402	8		NOR GATE
149	7486	9		EXCLUSIVE OR GATE
156	74107	10		J-K FLIP-FLOP
158	74161	11		BINARY COUNTER
161	9601	12		MULTIVIBRATOR
175	7474	13		D FLIP-FLOP
189	9322	14		MULTIPLEXER
194	74121	15		MULTIVIBRATOR
198	74123	16		MULTIVIBRATOR
200	7406	17		BUFFER DRIVER
201	7408	18		AND GATE
202	7403	19		NAND GATE
203	7405	20		INVERTER
204	7438	21		NAND BUFFER
206	7430	22		NAND GATE
207	7425	23		NOR GATE
208	7420	24		NAND GATE
2085	74S20	25		NAND GATE
209	7453	26		AND-OR-INVERT GATE
210	7437	27		NAND BUFFER
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213	7411	29		AND GATE
2135	74S11	30		AND GATE
224	7427	31		NOR GATE
241	7476	32		J-K FLIP-FLOP
2435	74S112	33		J-K FLIP-FLOP
500	74193	34		BINARY COUNTER
502	74180	35		PARITY GENERATOR
503	74160	36		DECADE COUNTER
505	74151	37		MULTIPLEXER
507	7442	38		DECIMAL DECODER
508	74153	39		MULTIPLEXER
518	74174	40		D FLIP-FLOP
520	74175	41		D FLIP-FLOP
521	7483	42		BINARY ADDER
524	7485	43		MAG COMPARATOR
527	74164	44		SHIFT REGISTER
531	74150	45		MULTIPLEXER
537	7493	46		BINARY COUNTER
540	74163	47		BINARY COUNTER
550	9314	48		LATCH FLIP-FLOP
551	7475	49		LATCH FLIP-FLOP
582	MC4024	50		MULTIVIBRATOR
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900	MC1488L	51A		LINE DRIVER
902	75154	51B		LINE RECEIVER
905	75451	52		AND DRIVER
981	7416	53		BUFFER DRIVER
	FC5	54		TERMINATOR
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	1667	56		NAND GATE
	1669	57		QUAD AMPLIFIER
772	2102	57A		RANDOM ACCESS MEMORY
	2518	58		SHIFT REGISTER
	TMS3113	59		ACCUMULATOR
	TMS3132	60		SHIFT REGISTER
	3401	61		OPERATIONAL LAMP
	MM5212	62		READ-ONLY MEMORY
	IM5603	63		READ-ONLY MEMORY
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227	7407	65		BUFFER DRIVER
943	7414	66		SCHMITT TRIGGER

ID #	VENDOR #	SHEET #	NETWORK #	DEVICE TYPE
968	7417	67		BUFFER DRIVER
218	7432	68		OR GATE
	7454	69		AND-OR INVERT GATE
548	7492	69A		BINARY COUNTER
216	74125	70		BUSS BUFFER GATE
167	74154	71		DECODER
	74LS158	72		MULTIPLEXER
547	74165	73		SHIFT REGISTER
	74173	74		D REGISTER
	74221	75		MULTIVIBRATOR
927	75453	76		OR DRIVER
	7812	76A		VOLTAGE REGULATOR
354G	7912	77		VOLTAGE REGULATOR
910	8820	78		LINE RECEIVER
909	8830	79		LINE DRIVER
	DRVR	80		LINE DRIVER
	RCVR	81		LINE RECEIVER
	DPLT	82		TRANSMITTER
	DPLR	83		RECEIVER
341	LM339	84		VOLTAGE COMPARITOR
	TR1602A	85		RECEIVER/TRANSMITTER
	6-60200	86		DRIVER
	6-60210	87		RECEIVER
780	8111	88		RAM
	74LS266	89		EXCLUSIVE NOR GATE
	74LS257	90		MULTIPLEXER
741S	MC1741S	91		OPERATIONAL AMP
	MPQ3725A	92	QN1	DRIVER TRANSISTOR
	2N6282-84	93	QN3	DARLINGTON CIRCUIT
	36C47	94	RN3	RESISTOR NETWORK
	MC3503L	95		OPERATIONAL AMP
	CD4066A	96		BILATERAL SWITCH
332	LM105H	97		VOLTAGE REGULATOR
	LM311	98		VOLTAGE COMPARATOR
	CA3094E	99		DIFFERENTIAL AMP
195	DM9602	100		MULTIVIBRATOR
	MC14415VP	101		TIMER/DRIVER
523	74192	102		BINARY COUNTER
	74136	103		EXCLUSIVE OR GATE
	2NG285-87	104		DARLINGTON CIRCUIT
916	555	105		TIMER
	MHQ3798	106	QN2	TRANSISTOR NETWORK
528	74194	107		SHIFT REGISTOR
	RS071675	108	RN4	RESISTOR NETWORK
	HA120975	109	RN5	RESISTOR NETWORK
	HA090475	110	RN6	RESISTOR NETWORK
	750	111	RN1	RESISTOR NETWORK
	750-81-R	112	RN2	RESISTOR NETWORK
	7905	113		VOLTAGE REGULATOR
936	556	114		TIMER
558	8080	115		LSI MICROPROCESSOR
	8224	116		CLOCK GEN & DRIVER
	8228	117		CONTROLLER & DRIVER
	8255	118		PROGRAM PERIPH IFACE
	8308	119		READ ONLY MEMORY
	8708	120		READ ONLY MEMORY
	8212	121		8 BIT I/O PORT
	8216	122		BI-DIR BUS DRIVER
	74LS174	123		FLIP-FLOP
	35391DC	124		ACCESS MEMORY
306	MC1747	125		OPERATIONAL AMP
4044	MC4044P	126		PHASE DETECTOR
	95359400-01	127	QN4	DARLINGTON CIRCUIT
	8251	128		PROGRAM COMM IFACE
	8214	129		PRIORITY IRUPT CONTROL
	44671763	130	RN7	RESISTOR NETWORK
	44671762	131	RN8	RESISTOR NETWORK

REV H

DWG NO C

SHEET 2A

CODE IDENT

KEY TO LOGIC SYMBOLS TITLE SHEET

TABLE OF CO NTENTS

ID #	VENDOR #	SHEET #	NETWORK #	DEVICE TYPE
	44671761	132	RN9	RESISTOR NETWORK
	44671764	133	RN10	RESISTOR NETWORK
	H11A5	134	DQN1	PHOTON COUPLED ISOLATER
	MD8002	135	QN11	NPN SILICON MUL TRAN
	44670963	136	DRN1	DIODE WITH 1 RES
	MOC80380	137		OPTIONAL COUPLER
146LS	74LS04	138		INVERTER
167LS	74LS154	139		DECODER
	75452	140		NAND DRIVER
218LS	74LS32	141		OR GATE
	74147	142		ENCODER
	750	143	RCN1	RESISTOR CAPACITOR NETWORK
	74LS14	144		SCHMITT TRIGGER
175LS	74LS74	145		JK FLIP FLOP
923	74132	146		NAND SCHMITT TRIGGER
	H11A5	147		PHOTO ISOLATER COUPLER
	7447A	148		DRIVER DECODER
	DL 707	149		NUMERIC LED DISPLAY
	44672798	150	RN 11	RESISTOR NETWORK
	44672797	151	RN 12	RESISTOR NETWORK
	44672528	152	RN13	RESISTOR NETWORK
	LM348/4741	153		OPERATIONAL AMP
	8748	154		8 BIT MICRO COMPUTER
	8048	155		8 BIT MICRO COMPUTER
	8085	156		8 BIT MICRO PROCESSOR
	8155	157		RAM, IO PORTS AND TIMER
	74LS155	158		MULTIPLEXER
	2114	159		RAM
	2716	160		ROM
	8355	161		ROM
	8755	162		EPROM
	2316E	163		ROM
	74145	164		DECODER
	745471	165		ROM
4490	MC14490	166		BOUNCE ELIMINATOR
5481	DS75492	167		DRIVER
74C922	MM74C922	168		DECODER
DC912	MM74C912	169		DISPLAY CONTROLLER

ID #	VENDOR #	SHEET #	NETWORK #	DEVICE TYPE

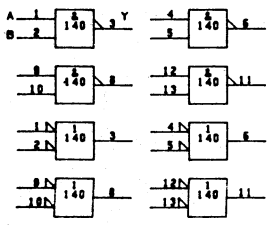
REV H

C

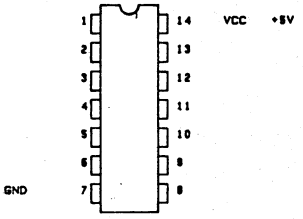
SHEET 2B

KEY TO LOGIC SYMBOLS TITLE SHEET

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	C 95387500
SHEET	9
CODE IDENT	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC $Y=\overline{AB}$

A	B	Y
1	1	0
0	1	1
1	0	1
0	0	1

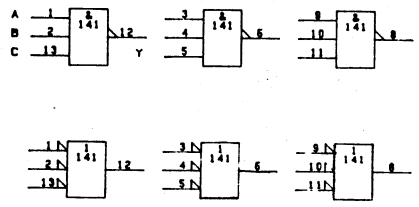
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADPRUPLE 2 INPUT TTL POSITIVE NAND GATE

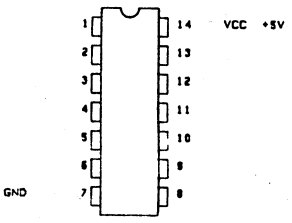
TIMING DIAGRAM

ELEMENT IDENTIFICATION 0140
VENDOR IDENTIFICATION 07400

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
DWG NO	95387500	
SIZE	C	SHEET 4
CODE IDENT		

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $Y=\overline{ABC}$

A	B	C	Y
1	1	1	0
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1

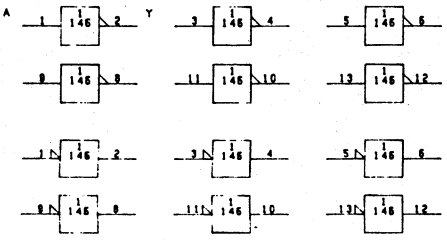
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TRIPLE 3-INPUT TTL POSITIVE NAND GATE

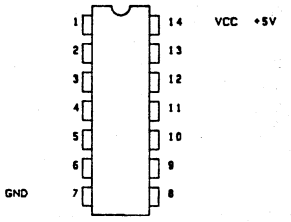
TIMING DIAGRAM

ELEMENT IDENTIFICATION #141
VENDOR IDENTIFICATION #7410

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE
POS LOGIC $Y=\overline{A}$

A	Y
0	1
1	0

GENERAL OPERATIONAL DESCRIPTION

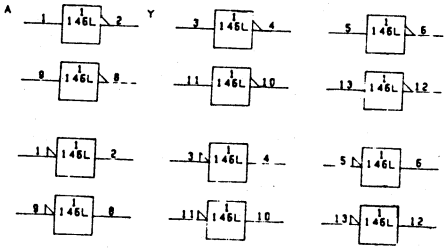
THIS DEVICE IS A TTL HEX INVERTER.

TIMING DIAGRAM

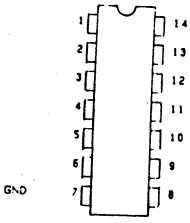
ELEMENT IDENTIFICATION #146
VENDOR IDENTIFICATION #7404

KEY TO LOGIC SYMBOLS
CODE IDENT C
DWG NO 95387500
REV A
SHEET 5

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET 6

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS LOGIC $Y=\overline{A}$

A	Y
0	1
1	0

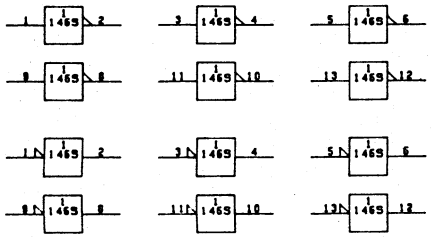
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A LOW-POWER TTL HEX INVERTER.

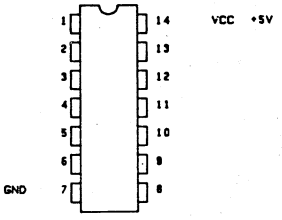
TIMING DIAGRAM

ELEMENT IDENTIFICATION #146L
VENDOR IDENTIFICATION #74L04

SYMBOL / APPLICATIONS / PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

CODE IDENT C DWG NO 95387500 SHEET 7

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC $Y=\overline{A}$

A	Y
0	1
1	0

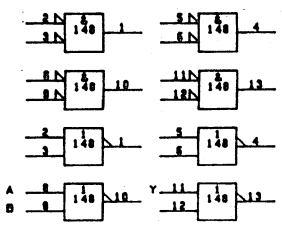
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A SCHOTTKY TTL HEX INVERTER.

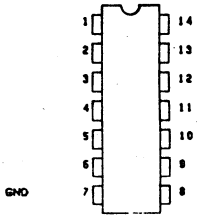
TIMING DIAGRAM

ELEMENT IDENDIFICATION #1465
VENDOR IDENTIFICATION #74S04

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET B

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $Y = \overline{A \cdot B}$

A	B	Y
1	0	0
0	1	0
1	1	0
0	0	1

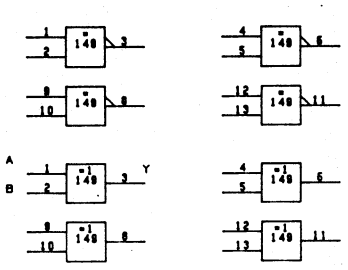
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE 2 INPUT TTL POSITIVE NOR GATE.

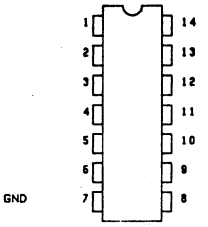
TIMING DIAGRAM

ELEMENT IDENTIFICATION #148
VENDOR IDENTIFICATION #7402

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	8

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $Y = A \otimes B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

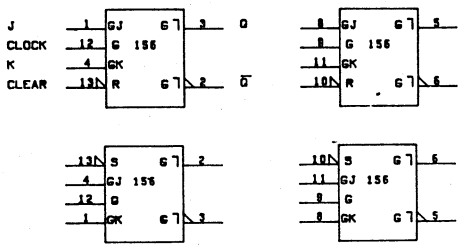
GENERAL OPERATIONAL DESCRIPTION

THIS QUADRUPLE 2 INPUT EXCLUSIVE-OR GATE UTILIZES TTL CIRCUITRY TO PERFORM THE FUNCTION $Y = A\bar{B} + \bar{A}B$. WHEN THE INPUT STATES ARE COMPLEMENTARY, THE OUTPUT GOES TO A LOGICAL 1.

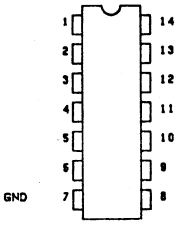
TIMING DIAGRAM

ELEMENT IDENTIFICATION #149
VENDOR IDENTIFICATION #7486

SYMBOL / APPLICATIONS / PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
DWG NO	95387500	
SHEET 10		
CODE IDENT	C	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

T_N		T_{N+1}	
J	K	Q	
0	0	Q_N	STAYS IN LAST STATE
0	1	0	
1	0	1	
1	1	$\overline{Q}_N$	TOGGLES WITH EACH CLOCK

NOTES--

1. T_N =BIT TIME BEFORE CLOCK PULSE.
2. T_{N+1}= BIT TIME AFTER CLOCK PULSE.
3. LOW INPUT TO CLEAR SETS Q TO LOGICAL 0. CLEAR IS INDEPENDENT OF CLOCK.

TIMING DIAGRAM

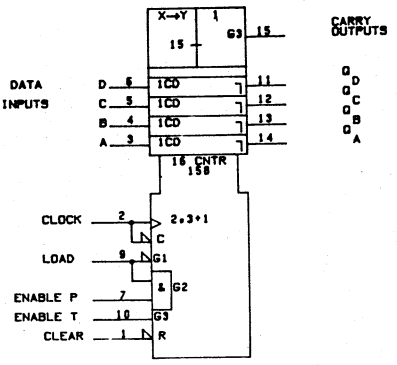
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL J-K FLIP-FLOP WITH COMPLEMENTARY Q AND $\overline{Q}$ OUTPUTS AND A DIRECT CLEAR (ALSO USABLE AS A DIRECT SET DEPENDING ON APPLICATION) INPUT. THESE J-K FLIP-FLOPS ARE BASED ON THE MASTER SLAVE PRINCIPLE. INPUTS TO THE MASTER SECTION ARE CONTROLLED BY THE CLOCK PULSE. THE CLOCK ALSO REGULATES THE STATE OF THE COUPLING TRANSISTORS WHICH CONNECT THE MASTER AND SLAVE SECTIONS. THE SEQUENCE OF OPERATION IS AS FOLLOWS...

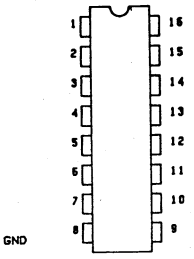
1. ISOLATE SLAVE FROM MASTER
2. ENTER INFORMATION FROM J AND K INPUTS TO MASTER
3. DISABLE J AND K INPUTS
4. TRANSFER INFORMATION FROM MASTER TO SLAVE.

ELEMENT IDENTIFICATION #156
VENDOR IDENTIFICATION #74107

SYMBOL / APPLICATION / PINS



MECHANICAL CONFIGURATION (TOP VIEW)



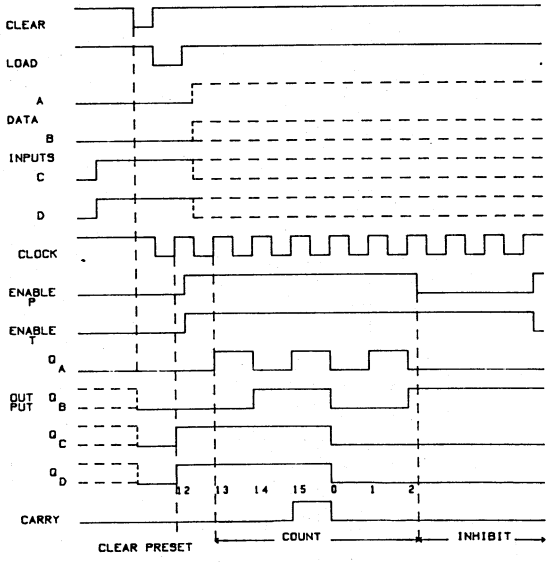
CODE IDENT	C	DWG NO	95387500
		SHEET	11

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC SEE DESCRIPTION

TIMING DIAGRAM
TYPICAL SEQUENCE OF OPERATION

1. CLEAR OUTPUT TO ZERO
2. PRESET TO BINARY THELVE
3. COUNT TO THIRTEEN, FOURTEEN, FIFTEEN, ZERO, ONE, AND TWO.
4. INHIBIT



GENERAL OPERATIONAL DESCRIPTION

THIS 4-BIT BINARY COUNTER IS A SYNCHRONOUS, PRE-SETABLE COUNTER WITH AN INTERNAL CARRY LOOK-AHEAD FOR APPLICATION IN HIGH-SPEED COUNTING SCHEMES. SYNCHRONOUS OPERATION IS PROVIDED BY HAVING ALL FLIP-FLOPS CLOCKED SIMULTANEOUSLY SO THAT THE OUTPUTS CHANGE COINCIDENT WITH EACH OTHER WHEN SO INSTRUCTED BY THE COUNT-ENABLE INPUT AND INTERNAL GATING. THE MODE OF OPERATION ELIMINATES THE OUTPUT COUNTING SPIKES WHICH ARE NORMALLY ASSOCIATED WITH ASYNCHRONOUS (RIPPLE CLOCK) COUNTERS. A BUFFERED CLOCK INPUT TRIGGERS THE FOUR J-K MASTER-SLAVE FLIP-FLOPS ON THE RISING (POSITIVE-GOING) EDGE OF THE CLOCK INPUT WAVEFORM.

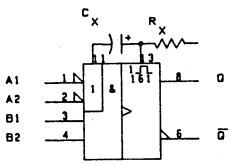
THIS COUNTER IS FULLY PROGRAMMABLE; THAT IS, THE OUTPUT MAY BE PRESET TO EITHER STATE. AS PRESETTING IS SYNCHRONOUS, PLACING A LOW LEVEL ON THE LOAD INPUT DISABLES THE COUNTER AND CAUSES THE OUTPUT TO AGREE WITH THE DATA INPUTS AFTER THE NEXT CLOCK PULSE. THE CLEAR FUNCTION IS ASYNCHRONOUS AND A LOW LEVEL AT THE CLEAR INPUT SET ALL FOUR OF THE FLIP-FLOP OUTPUTS TO A LOW REGARDLESS OF THE STATE OF THE CLOCK.

THE CARRY LOOK-AHEAD CIRCUITRY PROVIDES FOR CASCADING COUNTERS FOR N-BIT SYNCHRONOUS APPLICATIONS WITHOUT ADDITIONAL GATING.

INPUT CLOCK FREQUENCY IS 25 MEGAHERTZ MAXIMUM.

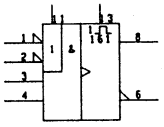
ELEMENT IDENTIFICATION #158
VENDOR IDENTIFICATION #74161

SYMBOL/APPLICATION/PINS

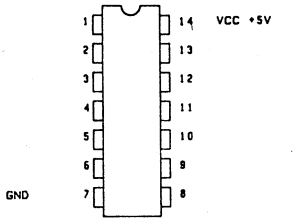


NOTE-- C_X AND R_X ARE EXTERNAL COMPONENTS.

OPTIONAL: RETRIGGERABLE MULTIVABRATOR ONE SHOT



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS

CODE IDENT	DWG NO	REV
C	95387500	H
	SHEET 12	

TRUTH TABLE
POS-LOGIC

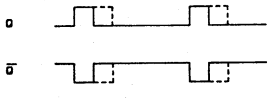
INPUT				OUTPUTS
A1	A2	B1	B2	Q AND $\overline{Q}$
H→L	H	H	H	ONE SHOT
H	H→L	H	H	ONE SHOT
L	X	L→H	H	ONE SHOT
X	L	L→H	H	ONE SHOT
L	X	H	L→H	ONE SHOT
X	L	H	L→H	ONE SHOT

T (TRIGGER) = $(\overline{A1} + \overline{A2}) \cdot B1 \cdot B2$

NOTES

1. A CHANGE OF T FROM FALSE TO TRUE CAUSES TRIGGER
2. H = HIGH VOLTAGE LEVEL
3. L = LOW VOLTAGE LEVEL
4. L → H = TRANSITION FROM LOW TO HIGH VOLTAGE LEVEL
5. H → L = TRANSITION FROM HIGH TO LOW VOLTAGE LEVEL
6. X = DON'T CARE (EITHER HIGH OR LOW VOLTAGE LEVEL)

TIMING DIAGRAM



GENERAL OPERATIONAL DESCRIPTION

THIS RETRIGGERABLE MONOSTABLE MULTIVIBRATOR HAS FOUR INPUTS. TWO ACTIVE HIGH AND TWO ACTIVE LOW. THIS ALLOWS A CHOICE OF LEADING EDGE OR TRAILING EDGE TRIGGERING. THE TTL INPUTS MAKE TRIGGERING INDEPENDENT OF INPUT TRANSITION TIMES.
WHEN INPUT CONDITIONS FOR TRIGGERING ARE MET, A NEW CYCLE STARTS AND THE EXTERNAL CAPACITOR IS RAPIDLY DISCHARGED AND THEN ALLOWED TO CHARGE. AN INPUT CYCLE TIME SHORTER THAN THE OUTPUT CYCLE TIME WILL RETRIGGER THE DEVICE AND RESULT IN A CONTINOUS TRUE OUTPUT RETRIGGERING MAY BE INHIBITED BY TYING THE NEGATION (Q) OUTPUT TO AN ACTIVE LOW INPUT. ACTIVE PULLUPS ARE PROVIDED ON THE OUTPUTS.
THE NOMINAL OUTPUT PULSE WIDTH IS DEFINED BY THE EQUATION

$$T = C_X \times R_X \times .32 \left(1 + \frac{.7K}{R_X}\right)$$

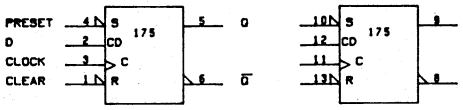
WHERE C_X = VALUE OF TIMING CAPACITOR

R_X = VALUE OF TIMING RESISTOR

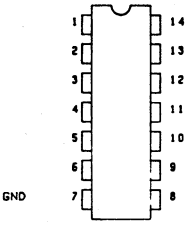
T = VALUE OF OUTPUT PULSE WIDTH

ELEMENT IDENTIFICATION #161
VENDOR IDENTIFICATION #8601

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
CODE IDENT	C
DWG NO	95387500
SHEET 13	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

T_N	T_{N+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES

1. T_N = BIT TIME BEFORE CLOOCK PULSE
2. T_{N+1} = BIT TIME AFTER CLOCK PULSE.
3. A LOW INPUT TO PRESET SETS Q TO LOGICAL 1.
   A LOW INPUT TO CLEAR SETS Q TO LOGICAL 0.
   THE PRESET AND CLEAR ARE INDEPENDENT OF THE CLOCK.

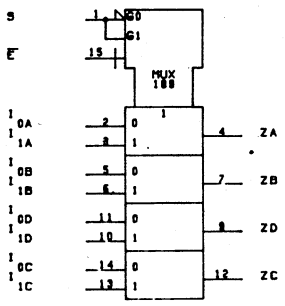
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

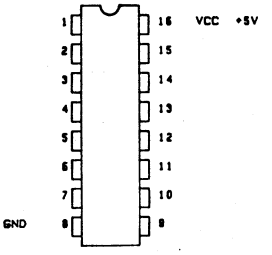
THESE MONOLITIC, DUAL, D-TYPE, EDGE TRIGGERED FLIP-FLOPS FEATURE DIRECT CLEAR AND PRESET INPUTS AND COMPLEMENTARY Q AND $\overline{Q}$ OUTPUTS. INPUT INFORMATION IS TRANSFERRED. TO THE OUTPUTS ON THE POSITIVE EDGE OF THE CLOCK PULSE. CLOCK TRIGGERING OCCURS AT A VOLTAGE LEVEL OF THE CLOCK PULSE AND IS NOT DIRECTLY RELATED TO THE TRANSITION TIME OF THE POSITIVE GOING PULSE. AFTER THE CLOCK INPUT THRESHOLD VOLTAGE HAS BEEN PASSED, THE DATA INPUT (D) IS LOCKED OUT.

ELEMENT IDENTIFICATION #175
VENDOR IDENTIFICATION #7474

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 14	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

ENABLE	SELECT INPUT	INPUTS		OUTPUTS
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H=HIGH LEVEL
L=LOW LEVEL
X=IRRELEVANT

THE ENABLE INPUT ($\overline{E}$) IS ACTIVE LOW. WHEN NOT ACTIVATED ALL OUTPUTS (Z) ARE LOW REGARDLESS OF ALL OTHER INPUTS.
THE LOGIC EQUATION FOR THE OUTPUT IS AS FOLLOWS.

$$Z_A = E \cdot (I_{1A} \cdot S + I_{0A} \cdot \overline{S})$$

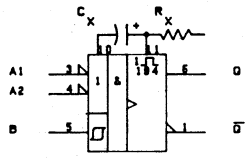
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

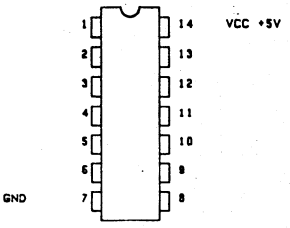
THIS TTL DEVICE IS A MONOLITHIC, TTL QUAD TWO-INPUT DIGITAL MULTIPLEXER CIRCUIT CONSISTING OF FOUR MULTIPLEXING CIRCUITS WITH COMMON SELECT AND ENABLE LOGIC. EACH CIRCUIT CONTAINS TWO INPUTS AND ONE OUTPUT WHEN THE ENABLE LINE IS LOW, DATA IS TRANSFERRED FROM THE INPUT SELECTED BY THE SELECT LINE TO THE OUTPUT.

ELEMENT IDENTIFICATION #189
VENDOR IDENTIFICATION #9322

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



NOTE-- C_X AND R_X ARE EXTERNAL COMPONENTS

KEY TO LOGIC SYMBOLS	CODE IDENT C	DWG NO 95387500	REV A
		SHEET 15	

TRUTH TABLE

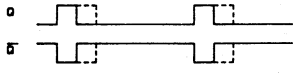
POS-LOGIC

T_N INPUT			T_{N+1} INPUT			OUTPUTS
A1	A2	B	A1	A2	B	Q AND $\overline{Q}$
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	0	1	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

NOTES-

1. T_N = TIME BEFORE INPUT TRANSITION.
2. T_{N+1} = TIME AFTER INPUT TRANSITION.
3. X INDICATES THAT EITHER A LOGICAL 0 OR 1 MAY BE PRESENT.
4. A1 AND A2 ARE NEGATIVE-EDGE TRIGGERED LOGIC INPUTS AND WILL TRIGGER THE ONE SHOT WHEN EITHER OR BOTH GO TO LOGICAL 0 WITH B AT A LOGICAL 1.
5. B IS A POSITIVE SCHMITT-TRIGGER INPUT FOR SLOW EDGES OR LEVEL DETECTION AND WILL TRIGGER THE ONE SHOT WHEN B GOES TO LOGICAL 1 WITH EITHER A1 OR A2 AT A LOGICAL 0.
6. TO USE THE INTERAL TIMING RESISTOR (2 K OHM NOM.) CONNECT PIN (9) TO PIN (14).
7. TO OBTAIN VARIABLE PULSE WIDTH CONNECT EXTERNAL VARIABLE RESISTANCE BETWEEN PIN (9) AND (14). NO EXTERNAL CURRENT LIMITING IS NEEDED.

TIMING DIAGRAM



GENERAL OPERATIONAL DESCRIPTION

THIS MONOLITHIC TTL MONOSTABLE MULTIVIBRATOR FEATURES D-C TRIGGERING FROM POSITIVE OR GATED NEGATIVE-GOING INPUT WITH INHIBIT FACILITY. PULSE TRIGGERING OCCURS AT A PARTICULAR VOLTAGE LEVEL AND IS NOT DIRECTLY RELATED TO THE TRANSITION TIME OF THE INPUT PULSE. SCHMITT-TRIGGER INPUT CIRCUITRY (TTL COMPATIBLE AND FEATURING TEMPERATURE-INDEPENDENT BACKLASH) FOR THE B INPUT ALLOWS JITTER-FREE TRIGGERING FROM THE INPUT WITH TRANSITION TIMES AS SLOW AS 1 VOLT/SECOND ONCE FIRED. THE OUTPUTS ARE INDEPENDENT OF FURTHER TRANSITIONS ON THE INPUT AND ARE A FUNCTION ONLY OF THE TIMING COMPONENTS. INPUT PULSES MAY BE OF ANY DURATION RELATIVE TO THE OUTPUT PULSE. OUTPUT PULSE LENGTHS MAY BE VARIED FROM 40 NANOSECONDS TO 40 SECONDS BY CHOOSING THE APPROPRIATE TIMING COMPONENTS. THE NOMINAL OUTPUT PULSE WIDTH IS DEFINED BY THE EQUATION

$$T = C_X \times R_X \times \log_E 2$$

WHERE C_X = VALUE OF TIMING CAPACITOR

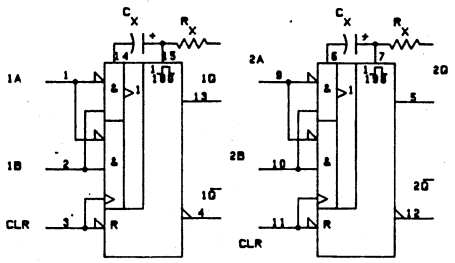
R_X = VALUE OF TIMING RESISTOR

T = VALUE OF OUTPUT PULSE WIDTH

ELEMENT IDENTIFICATION #194

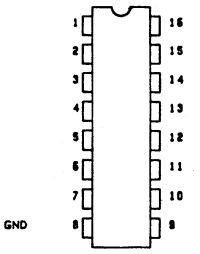
VENDOR IDENTIFICATION #74121

SYMBOL/APPLICATION/PINS



NOTE-- C_X AND R_X ARE EXTERNAL COMPONENTS

MECHANICAL CONFIGURATION (TOP VIEW)



REV	A		
DWG NO	C	95387500	
CODE IDENT			SHEET 16

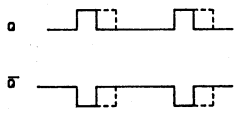
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUT		OUTPUT	
A	B	Q	Q̄
H	X	L	H
X	L	L	H
L	↑	⎍	⎍
↓	H	⎍	⎍

1. H = HIGH LEVEL (STEADY STATE)
2. L = LOW LEVEL (STEADY STATE)
3. ↑ = TRANSITION FROM LOW TO HIGH LEVEL
4. ↓ = TRANSITION FROM HIGH TO LOW LEVEL
5. ⎍ = ONE HIGH-LEVEL PULSE
6. ⎏ = ONE LOW-LEVEL PULSE
7. X = IRRELEVANT (ANY INPUT, INCLUDING TRANSITION)
8. LOW INPUT TO CLEAR RESETS Q TO LOW LEVEL AND INHIBITS DATA INPUTS

TIMING DIAGRAM



GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL MONOLITHIC RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH DC TRIGGERING FROM LOW LEVEL ACTIVE (A) INPUTS AND HIGH LEVEL ACTIVE (B) AND AN OVERRIDING DIRECT CLEAR INPUT. COMPLEMENTARY OUTPUTS ARE PROVIDED.
WHEN INPUT CONDITIONS FOR TRIGGERING ARE MET, A NEW CYCLE STARTS AND THE EXTERNAL CAPACITOR IS RAPIDLY DISCHARGED AND THEN ALLOWED TO CHARGE. AN INPUT CYCLE TIME SHORTER THAN THE OUTPUT CYCLE TIME WILL RETRIGGER THE DEVICE AND RESULT IN A CONTINOUS TRUE OUTPUT.
THE NOMINAL OUTPUT PULSE WIDTH IS DEFINED BY THE EQUATION

$$T = C_X \times R_X \times .28 \left(1 + \frac{.7K}{R_X}\right)$$

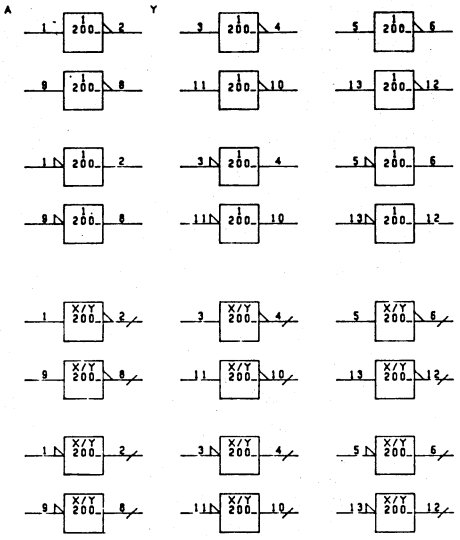
WHERE C_X = VALUE OF TIMING CAPACITOR

R_X = VALUE OF TIMING RESISTOR

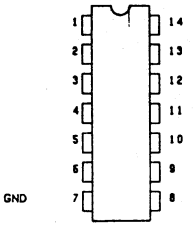
T = VALUE OF OUTPUT PULSE WIDTH

ELEMENT IDENTIFICATION #198
VENDOR IDENTIFICATION #74123

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE
POS LOGIC $Y=\bar{A}$

A	Y
1	0
0	1

GENERAL OPERATIONAL DESCRIPTION

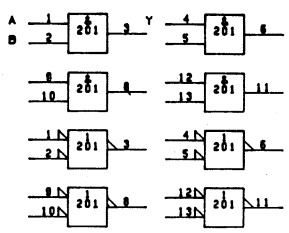
THIS DEVICE IS A TTL HEX INVERTER BUFFER/ DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS.

TIMING DIAGRAM

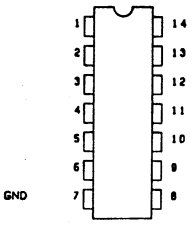
ELEMENT IDENTIFICATION #200
VENDOR IDENTIFICATION #7406

REV A
DWG NO 95387500
CODE IDENT C
SHEET 17
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	C 95387500
SHEET 18	
CODE IDENT	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC Y=AB

A	B	Y
1	1	1
0	1	0
1	0	0
0	0	0

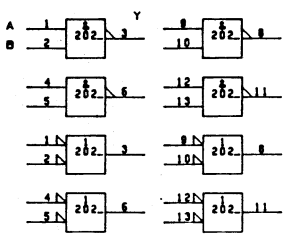
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE 2 INPUT POSITIVE AND GATE.

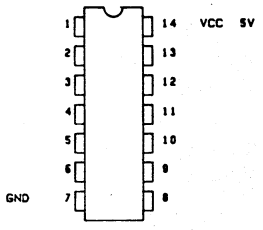
TIMING DIAGRAM

ELEMENT IDENTIFICATION #201
VENDOR IDENTIFICATION #7408

SYMBOLS/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	18

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $Y = \overline{AB}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

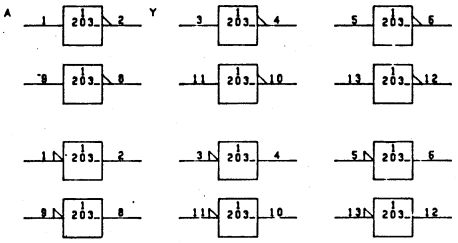
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE 2 INPUT POSITIVE TTL NAND GATE WITH OPEN COLLECTOR OUTPUTS.

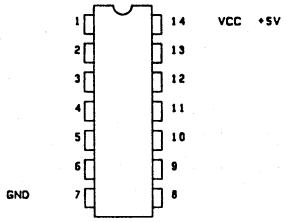
TIMING DIAGRAM

ELEMENT IDENTIFICATION #202
VENDOR IDENTIFICATION #7403

SYMBOL / APPLICATION / PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO C 95387500
SHEET 20
CODE IDENT
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC $Y=\overline{A}$

A	Y
0	1
1	0

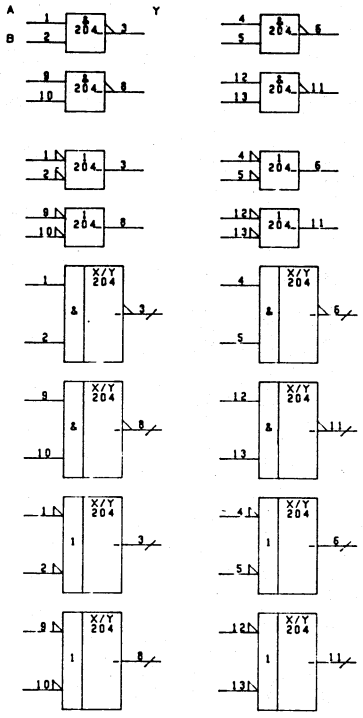
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TTL HEX INVERTER WITH OPEN COLLECTOR OUTPUTS.

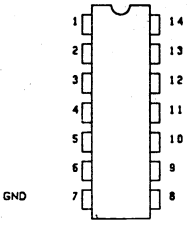
TIMING DIAGRAM

ELEMENT IDENTIFICATION #203
VENDOR IDENTIFICATION #7405

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 21	

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS LOGIC $Y=\overline{AB}$

A	B	Y
1	1	0
0	1	1
1	0	1
0	0	1

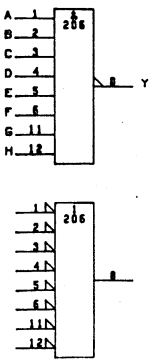
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE 2 INPUT TTL POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUTS.

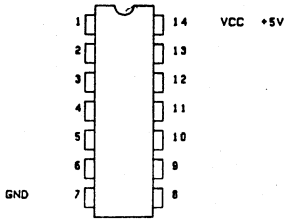
TIMING DIAGRAM

ELEMENT IDENTIFICATION #204
VENDOR IDENTIFICATION #7438

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A								
DWG NO	C	95387500							
SHEET 22									
CODE IDENT									

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS-LOGIC Y=$\overline{ABCDEFGH}$

A	B	C	D	E	F	G	H	Y
1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	1	1
0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	1	1
0	0	0	0	0	1	1	0	1
0	0	0	0	0	1	1	1	1
ETCETERA								⇕
1	1	1	1	1	1	1	0	1

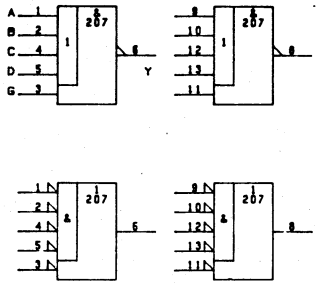
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

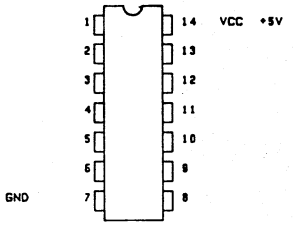
THIS DEVICE IS AN EIGHT INPUT TTL POSITIVE NAND GATE.

ELEMENT IDENTIFICATION #206
VENDOR IDENTIFICATION #7430

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS

REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	23

TRUTH TABLE
POS-LOGIC

$Y=\overline{G(A+B+C+D)}$

A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

H= HIGH LEVEL =1
L= LOW LEVEL =0
X= IRRELEVANT

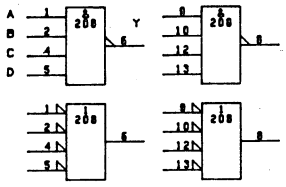
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL 4 INPUT TTL NOR GATE WITH STROBE.

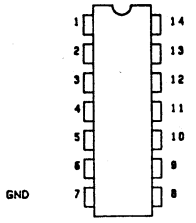
TIMING DIAGRAM

ELEMENT IDENTIFICATION #207
VENDOR IDENTIFICATION #7425

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
SHEET 24	
CODE IDENT	C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC $Y=\overline{ABCD}$

A	B	C	D	Y
1	1	1	1	0
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1

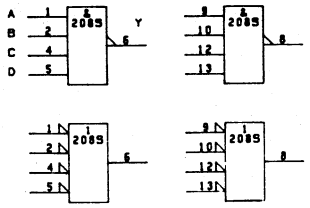
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

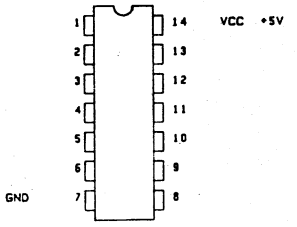
THIS DEVICE IS A DUAL 4 INPUT TTL POSITIVE NAND GATE.

ELEMENT IDENTIFICATION #208
VENDOR IDENTIFICATION #7420

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
DWG NO	95387500	SHEET 25
CODE IDENT	C	

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS-LOGIC $Y=\overline{ABCD}$

A	B	C	D	Y
1	1	1	1	0
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1

TIMING DIAGRAM

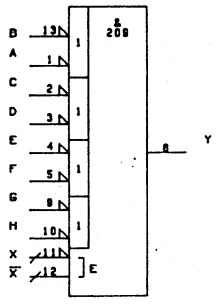
GENERAL OPERATIONAL DESCRIPTION

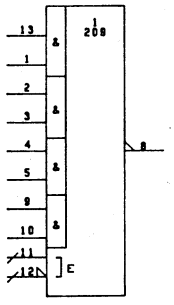
THIS DEVICE IS A DUAL 4 INPUT SCHOTTKY TTL POSITIVE NAND GATE.

ELEMENT IDENTIFICATION #2085

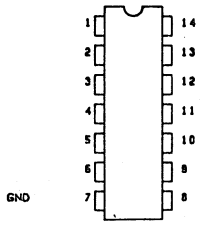
VENDOR IDENTIFICATION #74S20

SYMBOL/APPLICATION/PINS





MECHANICAL CONFIGURATION (TOP VIEW)



CSV	A
CODE IDENT	C
DWG NO	95387500
SHEET 28	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $Y = \overline{(AB)+(CD)+(EF)+(GH)+(X)}$

A	B	C	D	E	F	G	H	X	$\overline{X}$	Y
0	X	0	X	0	X	0	X	0	1	1
X	0	X	0	X	0	X	0	0	1	1
1	1	X	X	X	X	X	X	X	X	0
X	X	1	1	X	X	X	X	X	X	0
X	X	X	X	1	1	X	X	X	X	0
X	X	X	X	X	X	1	1	X	X	0
X	X	X	X	X	X	X	X	1	0	0
ETCETRA										

X= IRRELEVANT

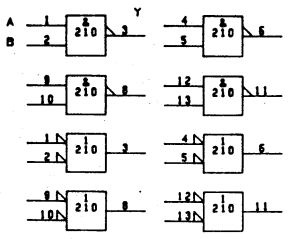
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A 4 WIDE 2 INPUT TTL AND-OR-INVERT GATE WITH EXTENDER INPUTS. A TOTAL OF 4 EXPANDER GATES CAN BE CONNECTED TO THE EXPANDER INPUTS. IF NO EXPANDER GATES ARE USED X AND $\overline{X}$ ARE LEFT OPEN.

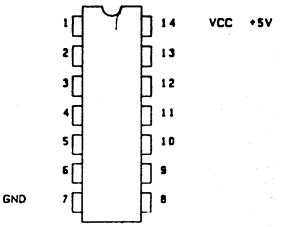
TIMING DIAGRAM

ELEMENT IDENTIFICATION #208
VENDOR IDENTIFICATION #7453

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 27	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $Y = \overline{AB}$

A	B	Y
1	1	0
0	1	1
1	0	1
0	0	1

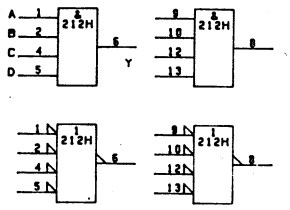
OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE 2 INPUT TTL POSITIVE NAND BUFFER.

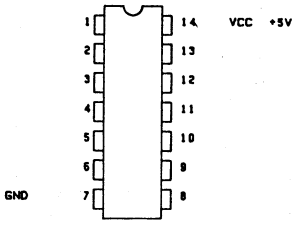
TIMING DIAGRAM

ELEMENT IDENTIFICATION #210
VENDOR IDENTIFICATION #7437

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
SHEET 28	
CODE IDENT	C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC Y= ABCD

A	B	C	D	Y
1	1	1	1	1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0

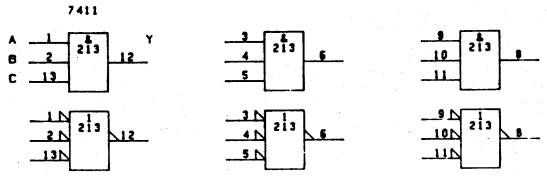
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL 4 INPUT HIGH SPEED TTL POSITIVE AND GATE.

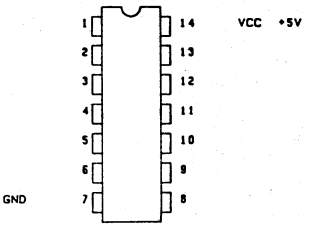
TIMING DIAGRAM

ELEMENT IDENTIFICATION #212H
VENDOR IDENTIFICATION #74H21

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

CODE IDENT	DWG NO	SHEET
C	9538750,0	28

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC Y= ABC

A	B	C	Y
1	1	1	1
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0

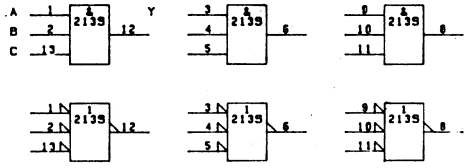
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TRIPLE 3 INPUT TTL POSITIVE AND GATE.

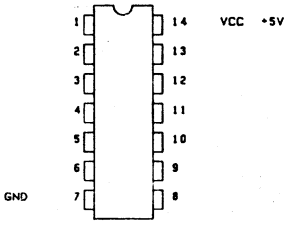
TIMING DIAGRAM

ELEMENT IDENTIFICATION #213
VENDOR IDENTIFICATION #7411

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET 30

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS-LOGIC Y= ABC

A	B	C	Y
1	1	1	1
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0

GENERAL OPERATIONAL DESCRIPTION

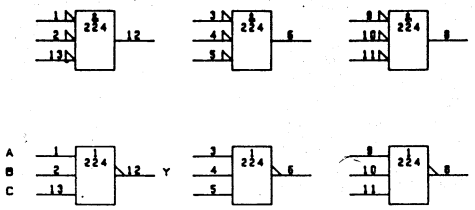
THIS DEVICE IS A TRIPLE 3 INPUT TTL POSITIVE AND GATE.

TIMING DIAGRAM

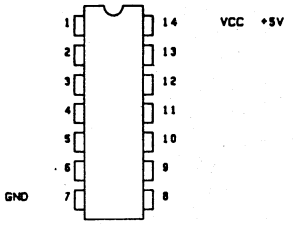
ELEMENT IDENTIFICATION #2139

VENDOR IDENTIFICATION #7491:

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET 31

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS LOGIC $Y = \overline{A \cdot B \cdot C}$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

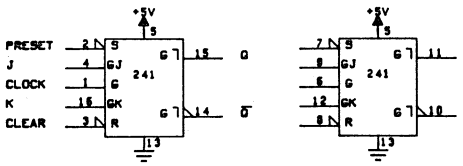
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TRIPLE 3 INPUT TTL POSITIVE NOR GATE.

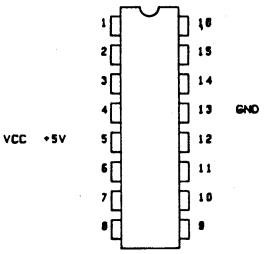
TIMING DIAGRAM

ELEMENT IDENTIFICATION #224
VENDOR IDENTIFICATION #7427

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
DWG NO	95387500	
CODE IDENT	C	SHEET 32

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

T_N		T_{N+1}	
J	K	Q	
0	0	Q_N	STAYS IN LAST STATE
0	1	0	
1	0	1	
1	1	$\overline{Q}_N$	TOGGLES WITH EACH CLOCK

NOTES--

1. T_N = BIT TIME BEFORE CLOCK PULSE.
2. T_{N+1} = BIT TIME AFTER CLOCK PULSE.
3. LOW INPUT TO PRESET SETS Q TO LOGICAL 1
   LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
   CLEAR AND PRESET ARE INDEPENDENT OF CLOCK

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL J-K FLIP FLOP WITH COMPLEMENTARY Q AND $\overline{Q}$ OUTPUTS AND PRESET AND CLEAR INPUTS. THE DEVICE IS BASED ON THE MASTER SLAVE PRINCIPLE. INPUTS TO THE MASTER SECTION ARE CONTROLLED BY THE CLOCK PULSE. THE CLOCK PULSE ALSO REGULATES THE STATE OF THE COUPLING TRANSISTORS WHICH CONNECT THE MASTER AND SLAVE SECTIONS. THE SEQUENCE OF OPERATION IS AS FOLLOWS--

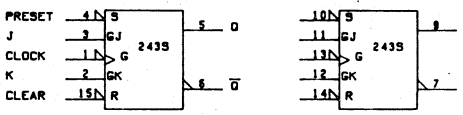
1. ISOLATE SLAVE FROM MASTER
2. ENTER INFORMATION FROM J AND K INPUTS TO MASTER.
3. DISABLE J AND K INPUTS.
4. TRANSFER INFORMATION FROM MASTER TO SLAVE

INPUT IS TRANSFERRED ON LEADING EDGE OF CLOCK
OUTPUT IS TRANSFERRED ON TRAILING EDGE OF CLOCK

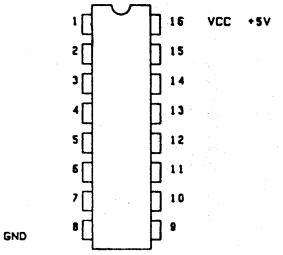
TIMING DIAGRAM

ELEMENT IDENTIFICATION #241
VENDOR IDENTIFICATION #7476

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 33	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

T_N J	T_N K	T_{N+1}	
J	K	Q	
L	L	Q_N	STAYS IN LAST STATE
L	H	L	
H	L	H	
H	H	$\overline{Q}_N$	TOGGLES WITH EACH CLOCK

1. T_N = BIT TIME BEFORE CLOCK PULSE
2. T_{N+1} = BIT TIME AFTER CLOCK PULSE
3. LOW INPUT TO PRESET SETS Q TO HIGH LEVEL
   LOW INPUT TO CLEAR RESETS Q TO LOW LEVEL
   CLEAR AND PRESET ARE INDEPENDANT OF CLOCK

GENERAL OPERATIONAL DESCRIPTION

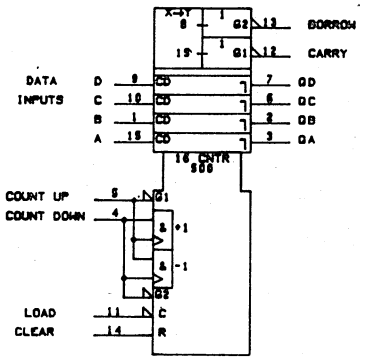
THIS DEVICE IS A DUAL JK FLIP-FLOP WITH INDIVIDUAL J,K, CLOCK, AND ASYNCHRONOUS PRESET AND CLEAR INPUTS TO EACH FLIP-FLOP. WHEN THE CLOCK GOES HIGH, THE INPUTS ARE ENABLED AND DATA WILL BE ACCEPTED. THE LOGIC LEVEL OF THE J AND K INPUTS WILL BE ALLOWED TO CHANGE WHEN THE CLOCK PULSE IS HIGH AND THE BISTABLE MULTIVIBRATOR WILL PERFORM ACCORDING TO THE TRUTH TABLE AS LONG AS MINIMUM SETUP AND HOLD TIMES ARE OBSERVED. INPUT DATA IS TRANSFERRED TO THE OUTPUTS ON THE NEGATIVE GOING EDGE OF THE CLOCK PULSE.

T SETUP MIN. = 3 NANO SEC.
T HOLD MIN. = 0 NANO SEC.
MAXIMUM INPUT CLOCK FREQUENCY IS 80 MEGAHERTZ.

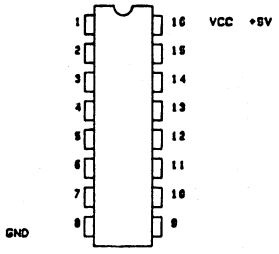
TIMING DIAGRAM

ELEMENT IDENTIFICATION #2435
VENDOR IDENTIFICATION #74S112

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)

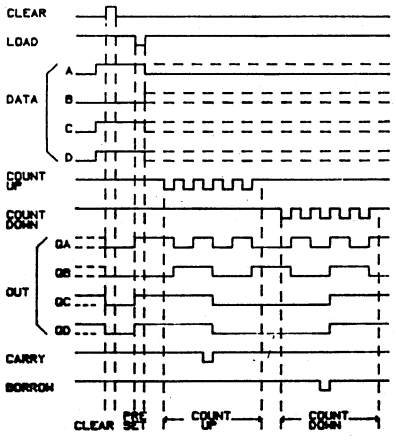


KEY TO LOGIC SYMBOLS	CODE IDENT C	DWG NO 95387500	REV A
		SHEET 34	

TRUTH TABLE
POS-LOGIC
LOW INPUT TO LOAD SET

Q_A = A
Q_B = B
Q_C = C
Q_D = D

TIMING DIAGRAM
CLEAR-LOAD-AND COUNT SEQUENCE



GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A SYNCRONOUS 4-BIT BINARY UP-DOWN COUNTER. SYNCHRONOUS OPERATION IS PROVIDED BY HAVING ALL FLIP-FLOPS CLOCKED SIMULTANEOUSLY SO THAT THE OUTPUTS CHANGE COINCIDENTLY WITH EACH OTHER WHEN SO INSTRUCTED BY THE STEERING LOGIC. THE OUTPUT OF THE FOUR MASTER-SLAVE FLIP-FLOPS ARE TRIGGERED BY A LOW-TO-HIGH TRANSITION OF EITHER COUNT (CLOCK) INPUT. THE DIRECTION OF COUNTING IS DETERMINED BY WHICH COUNT INPUTS IS PULSED WHILE THE OTHER COUNT INPUT IS HIGH.

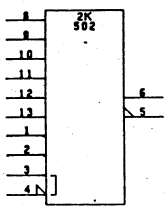
THIS COUNTER IS FULLY PROGRAMMABLE. THAT IS THE OUTPUT MAY BE PRESET TO ANY STATE BY ENTERING THE DESIRED DATA AT THE DATA INPUT WHILE THE LOAD INPUT IS LOW. THE OUTPUT WILL CHANGE TO AGREE WITH THE DATA INPUTS INDEPENDENTLY OF THE COUNT PULSES. WHEN A HIGH LEVEL IS APPLIED TO THE CLEAR INPUT IT WILL FORCE ALL OUTPUTS TO THE LOW LEVEL.

BOTH BORROW AND CARRY OUTPUTS ARE AVAILABLE TO CASCADE BOTH THE UP AND DOWN COUNTING FUNCTIONS. THE BORROW OUTPUT PRODUCES A PULSE EQUAL IN WIDTH TO HTE COUNT-DOWN INPUT WHEN THE COUNTER UNDERFLOWS. SIMILARLY, THE CARRY OUTPUT PRODUCES A PULSE EQUAL IN WIDTH TO THE COUNT-UP INPUT WHEN AN OVERFLOW CONDITION EXISTS.

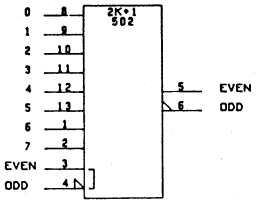
MAXIMUM INPUT COUNT FREQUENCY IS 25 MEGAHERTZ.

THE CLEAR FUNCTION IS INDEPENDENT OF THE COUNT & LOAD INPUTS.
ELEMENT IDENTIFICATION #500
VENDOR IDENTIFICATION #74193

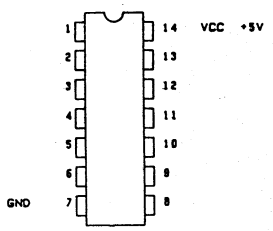
SYMBOL/APPLICATION/PINS



INPUTS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO C 95387500
SHEET 38
CODE IDENT
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUTS			OUTPUTS	
Σ OF 1'S AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X= IRRELEVANT

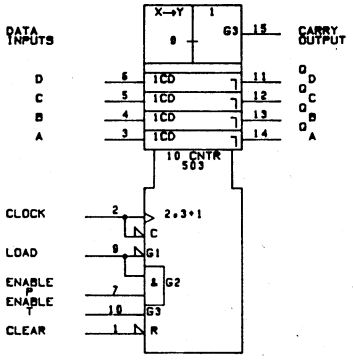
GENERAL OPERATIONAL DESCRIPTION

THIS UNIVERSAL, MONOLITHIC, 8 BIT PARITY GENERATOR CHECKER. HAS ODD/EVEN OUTPUTS AND CONTROL INPUTS TO FACILITATE OPERATION IN EITHER ODD OR EVEN PARITY APPLICATIONS. THE WORD LENGTH CAPABILITY CAN BE EXPANDED BY CASCADING.

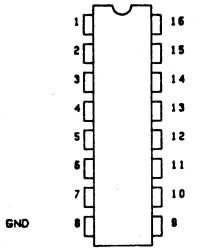
TIMING DIAGRAM

ELEMENT IDENTIFICATION #502
VENDOR IDENTIFICATION #74180

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



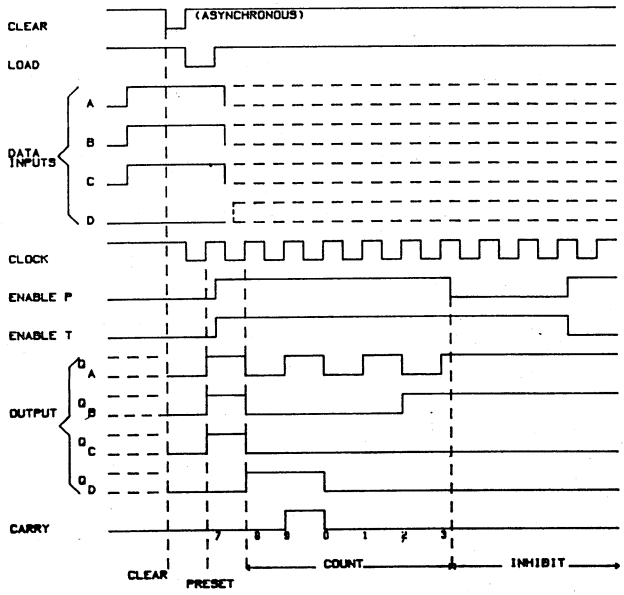
REV	A
DWG NO	95387500
SHEET 36	
CODE IDENT	C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC SEE DESCRIPTION

TIMING DIAGRAM
TYPICAL SEQUENCE OF OPERATION

1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BCD SEVEN
3. COUNT TO EIGHT,NINE,ZERO,ONE,TWO,AND THREE
4. INHIBIT

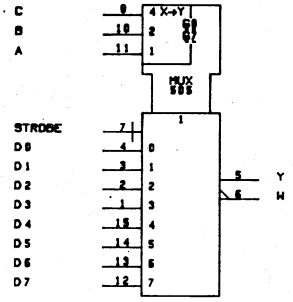


GENERAL OPERATIONAL DESCRIPTION

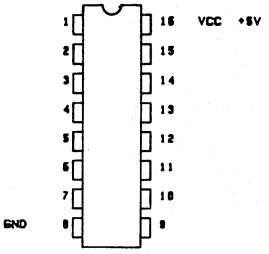
THIS SYNCHRONOUS, PRESETTABLE COUNTER HAS AN INTERNAL CARRY LOOK-AHEAD FOR APPLICATION IN HIGH SPEED COUNTING SCHEMES. THIS DECADE COUNTER PROVIDES SYNCHRONOUS OPERATION BY HAVING ALL FLIP-FLOPS CLOCKED SIMULTANEOUSLY SO THAT THE OUTPUTS CHANGE COINCIDENT WITH EACH OTHER WHEN SO INSTRUCTED BY THE COUNT-ENABLE INPUTS AND INTERNAL GATING.
THESE COUNTERS ARE FULLY PROGRAMMABLE; THAT IS, THE OUTPUTS MAY BE PRESET TO EITHER STATE. AS PRESETTING IS SYNCHRONOUS, PLACING A LOW LEVEL ON THE LOAD INPUT DISABLES THE COUNTER AND CAUSES THE OUTPUTS TO AGREE WITH THE DATA INPUTS AFTER THE NEXT CLOCK PULSE. THIS CLEAR FUNCTION IS ASYNCHRONOUS AND A LOW LEVEL AT THE CLEAR INPUT SETS ALL FOUR OF THE FLIP-FLOP OUTPUTS LOW REGARDLESS OF THE STATE OF THE CLOCK.
THE CARRY LOOK-AHEAD CIRCUITRY PROVIDES FOR CASCADING COUNTERS FOR N-BIT SYNCHRONOUS APPLICATION WITHOUT ADDITIONAL GATING. INSTRUMENTAL IN ACCOMPLISHING THIS FUNCTION ARE TWO COUNT-ENABLE INPUTS AND A CARRY OUTPUT. BOTH COUNT-ENABLE INPUTS (P AND T) MUST BE HIGH TO COUNT, AND INPUT T IS FED FORWARD TO ENABLE THE CARRY OUTPUT. THE CARRY OUTPUT THUS ENABLED WILL PRODUCE A POSITIVE OUTPUT PULSE WITH A DURATION APPROXIMATELY EQUAL TO THE POSITIVE PORTION OF THE Q_A OUTPUT. THIS POSITIVE OVERFLOW CARRY PULSE CAN BE USED TO ENABLE SUCCESSIVE CASCADED STAGES. HIGH-TO-LOW-LEVEL TRANSITIONS AT THE ENABLE P OR T INPUTS SHOULD OCCUR ONLY WHEN THE CLOCK INPUT IS HIGH.
MAXIMUM CLOCK FREQUENCY IS 25 MEGAHERTZ

ELEMENT IDENTIFICATION #503
VENDOR IDENTIFICATION #74160

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE
POS-LOGIC

INPUTS												OUTPUTS	
C	B	A	STROBE (1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y (1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

X= IRRELEVANT

TIMING DIAGRAM

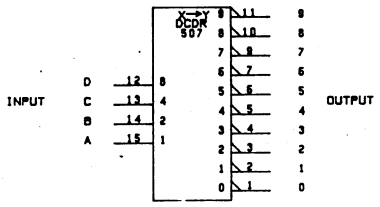
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A 8 LINE TO 1 LINE DATA SELECTOR/MULTIPLEXER WITH STROBE. WHEN THE STROBE LINE IS LOW, DATA IS TRANSFERRED FROM THE INPUT SELECTED BY THE DATA SELECT LINES TO THE OUTPUT (NOTE THAT COMPLIMENTRY Y AND W OUTPUTS ARE PROVIDED).

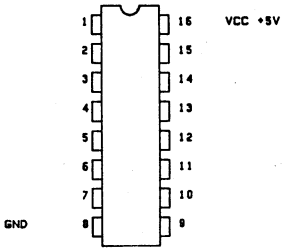
ELEMENT IDENTIFICATION #505
VENDOR IDENTIFICATION # 74151

REV A
DWG NO 95387500
CODE IDENT C
SHEET 37
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS

CODE IDENT C DWG NO 95387500 REV A SHEET 38

TRUTH TABLE
POS LOGIC

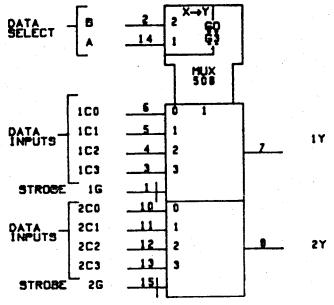
BCD INPUTS				DECIMAL OUTPUT									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

GENERAL OPERATIONAL DESCRIPTION

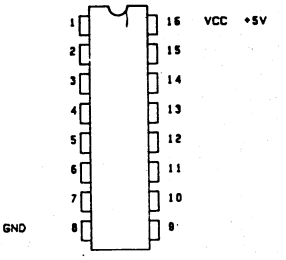
THIS MONOLITHIC DECIMAL DECODER CONSISTS OF EIGHT INVERTERS AND TEN FOUR-INPUT NAND GATES. THE INVERTERS ARE CONNECTED IN PAIRS TO MAKE BCD INPUT DATA AVAILABLE FOR DECODING BY THE NAND GATES. FULL DECODING OF VALID INPUT LOGIC ENSURES THAT ALL OUTPUTS REMAIN OFF FOR ALL INVALID INPUT CONDITIONS.
A VALID BCD INPUT WILL ENABLE ONE OF THE OUTPUTS AS INDICATED.

ELEMENT IDENTIFICATION #507
VENDOR IDENTIFICATION #7442

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
CODE IDENT	C
DWG NO	95387500
SHEET	38

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

DATA SELECTS B	A	DATA INPUTS C0	C1	C2	C3	STROBE G	OUTPUT Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H= HIGH LEVEL
L= LOW LEVEL
X= IRRELEVANT

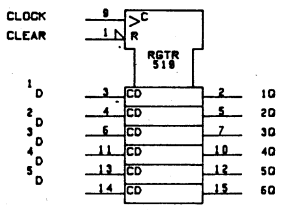
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

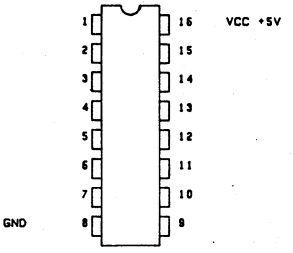
THIS DEVICE IS A DUAL 4 LINE TO 1 LINE DATA SELECTOR/MULTIPLEXER. THE DEVICES HAVE INDEPENDENT STROBE LINES, BUT SHARE COMMON DATA SELECT LINES. WHEN THE STROBE LINE IS LOW, DATA IS TRANSFERED FROM THE INPUT SELECTED BY THE DATA SELECT LINES TO THE OUTPUT.

ELEMENT IDENTIFICATION #508
VENDOR IDENTIFICATION #74153

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET 40

CODE IDENT C

KEY TO LOGIC SYMBOLS

GENERAL OPERATIONAL DESCRIPTION

THIS MONOLITHIC POSITIVE-EDGE-TRIGGERED FLIP-FLOP UTILIZES TTL CIRCUITRY TO IMPLEMENT D TYPE FLIP-FLOP LOGIC.
INFORMATION AT THE D INPUT MEETING THE SETUP TIME REQUIREMENTS IS TRANSFERRED TO THE Q OUTPUTS ON THE POSITIVE-GOING EDGE OF THE CLOCK PULSE. CLOCK TRIGGERING OCCURS AT A PARTICULAR VOLTAGE LEVEL AND IS NOT DIRECTLY RELATED TO THE TRANSITION TIME OF THE POSITIVE-GOING PULSE. WHEN THE CLOCK INPUT IS AT EITHER THE HIGH OR LOW LEVEL, THE D INPUT SIGNAL HAS NO EFFECT AT THE OUTPUT. THIS DEVICE FEATURES SIX FLIP-FLOPS WITH A COMMON DIRECT CLEAR.

TRUTH TABLE
POS LOGIC

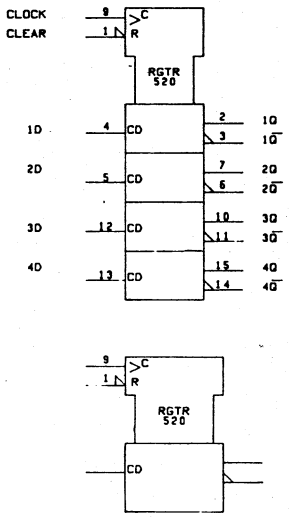
INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT
↑ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.

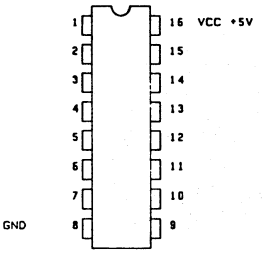
TIMING DIAGRAM

ELEMENT IDENTIFICATION #519
VENDOR IDENTIFICATION #74174

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO 95387500
SHEET 41
CODE IDENT C
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

1. H=HIGH LEVEL (STEADY STATE)=1
2. L=LOW LEVEL (STEADY STATE)=0
3. X=IRRELEVANT
4. ↑ =TRANSITION FROM LOW TO HIGH LEVEL
5. Q_0=THE LEVEL OF Q BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED.

TIMING DIAGRAM

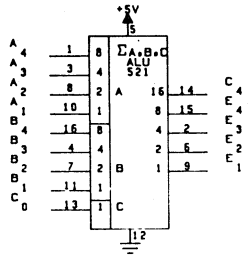
GENERAL OPERATIONAL DESCRIPTION

THESE MONOLITHIC, POSITIVE-EDGE-TRIGGERED FLIP-FLOPS UTILIZE TTL CIRCUITRY TO IMPLEMENT D-TYPE FLIP-FLOP LOGIC. ALL HAVE DIRECT CLEAR INPUT, AND FEATURE COMPLEMENTARY OUTPUT FROM EACH FLIP-FLOPS.

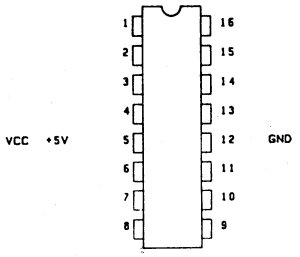
INFORMATION AT THE D INPUT MEETING THE SETUP TIME REQUIREMENTS IS TRANSFERRED TO THE Q OUTPUT ON THE POSITIVE-GOING EDGE OF THE CLOCK PULSE. CLOCK TRIGGERING OCCURS AT A PARTICULAR VOLTAGE LEVEL AND IS NOT DIRECTLY RELATED TO THE TRANSITION TIME OF THE POSITIVE-GOING PULSE. WHEN THE CLOCK INPUT IS AT EITHER THE HIGH OR LOW THE D INPUT SIGNAL HAS NO EFFECT AT THE OUTPUT.

ELEMENT IDENTIFICATION #520
VENDOR IDENTIFICATION #74175

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	C 95387500
SHEET 42	
CODE IDENT	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUT				OUTPUT					
				WHEN $C_0=0$			WHEN $C_0=1$		
				WHEN $C_2=0$			WHEN $C_2=1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

1. INPUT CONDITIONS $A+A_1$, B_1, B_2, AND C_0 ARE USED TO DETERMINE OUTPUTS Σ_1 AND Σ_2, AND THE VALUE OF THE INTERNAL CARRY C_2. THE VALUES AT C_2, A_3, B_3, A_4, AND B_4 ARE THEN USED TO DETERMINE OUTPUTS Σ_3, Σ_4, AND C_4.
2. C2 IS AN INTERNAL ADDER CARRY.

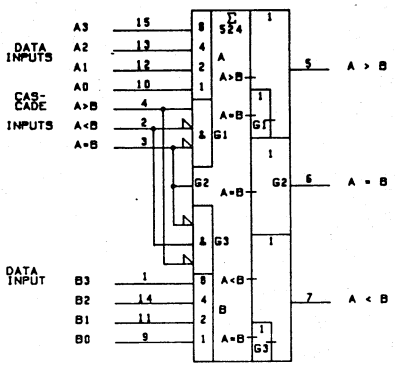
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

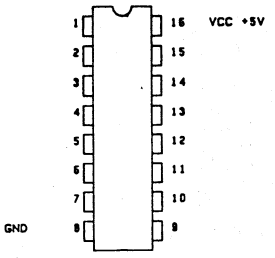
THIS DEVICE IS A 4-BIT BINARY FULL ADDER WITH CARRY. IT PERFORMS THE ADDITION OF TWO 4 BIT BINARY NUMBERS. THE SUM (E) OUTPUTS ARE PROVIDED FOR EACH BIT AND THE RESULTANT CARRY (C_4) IS OBTAINED FROM THE FOURTH BIT.

ELEMENT IDENTIFICATION #521
VENDOR IDENTIFICATION #7483

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO 95387500
CODE IDENT C
SHEET 43

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

H = HIGH LEVEL
L = LOW LEVEL
X = IRRELEVANT

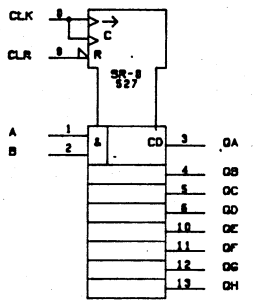
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

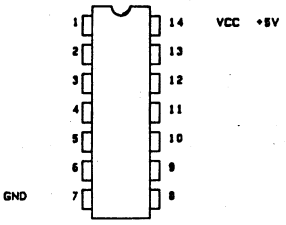
THIS DEVICE IS A 4 BIT MAGNITUDE COMPARATOR. IT PERFORMS MAGNITUDE COMPARISON OF STRAIGHT BINARY AND STRAIGHT BCD (8421) CODES. THREE FULLY DECODED DECISIONS ABOUT TWO 4-BIT WORDS (A, B) ARE MADE AND ARE EXTERNALLY AVAILABLE AT THREE OUTPUTS. THESE DEVICES ARE FULLY EXPANDABLE TO ANY NUMBER OF BITS WITHOUT EXTERNAL GATES. WHEN CASCADED, THE TOTAL TIME FOR COMPARISON IS THE FUNCTION OF THE WORD LENGTH, HOWEVER, ONLY A TWO-GATE-LEVEL DELAY (12 NS) IS ADDED FOR EACH FOUR-BIT EXPANSION

ELEMENT IDENTIFICATION #524
VENDOR IDENTIFICATION #7485

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
SHEET 44	
CODE IDENT	C

KEY TO LOGIC SYMBOLS

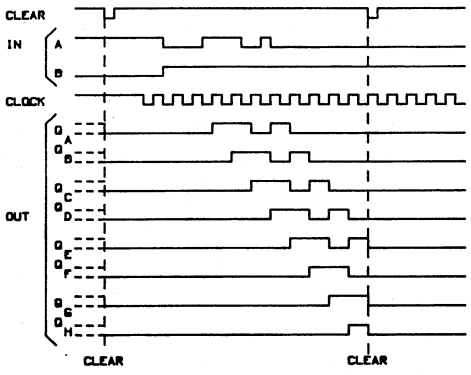
TRUTH TABLE
POS LOGIC SERIAL INPUTS A AND B

INPUTS AT TN		OUTPUTS AT TN+1
A	B	QA
H	H	H
L	H	L
H	L	L
L	L	L

GENERAL OPERATIONAL DESCRIPTION

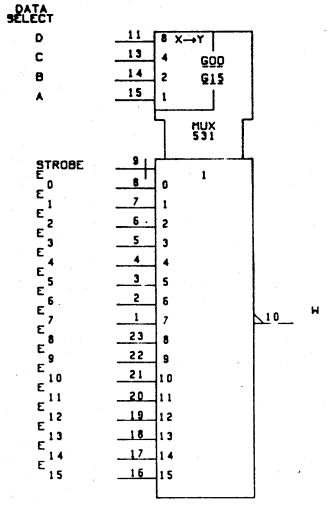
THIS 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER HAS 2 GATE SERIAL INPUTS AND AN ASYNCHRONOUS CLEAR. THE GATED SERIAL INPUTS (A AND B) PERMIT COMPLETE CONTROL OVER INCOMING DATA AS A LOW AT EITHER (OR BOTH) INPUT (S) INHIBITS ENTRY OF THE NEW DATA AND RESETS THE FIRST FLIP-FLOP TO THE LOW LEVEL AT THE NEXT CLOCK PULSE. A HIGH-LEVEL INPUT ENABLES THE OTHER INPUT WHICH WILL THEN DETERMINE THE STATE OF THE FIRST FLIP FLOP. DATA AT THE SERIAL INPUTS MAY BE CHANGED WHILE THE CLOCK IS HIGH, BUT ONLY INFORMATION MEETING THE SETUP REQUIREMENTS WILL BE ENTERED. CLOCKING OCCURS ON THE LOW-TO-HIGH LEVEL TRANSITION OF THE CLOCK INPUT.
MAXIMUM INPUT CLOCK FREQUENCY IS 25 MEGAHERTZ.

TIMING DIAGRAM
CLEAR-INHIBIT-SHIFT-CLEAR AND INHIBIT SEQUENCE

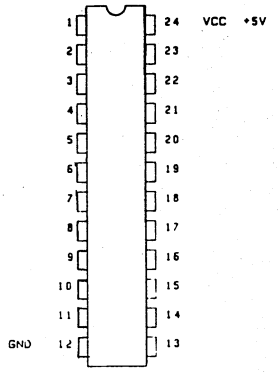


ELEMENT IDENTIFICATION #527
VENDOR IDENTIFICATION #74164

SYMBOL APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

CODE IDENT C

SHEET 45

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

INPUTS																			OUTPUT
D	C	B	A	STROBE	E 0	E 1	E 2	E 3	E 4	E 5	E 6	E 7	E 8	E 9	E 10	E 11	E 12	E 13	E 14	E 15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

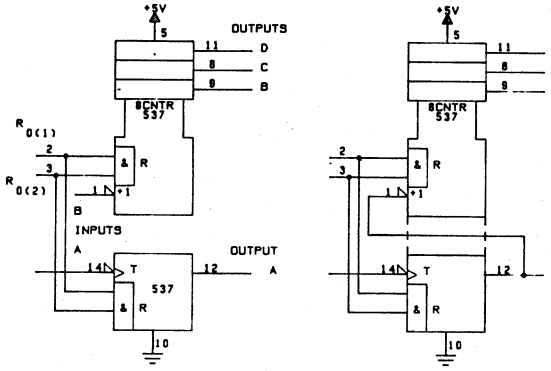
WHEN USED TO INDICATE AN INPUT CONDITION, X= LOGICAL 1 OR LOGICAL 0

GENERAL OPERATIONAL DESCRIPTION

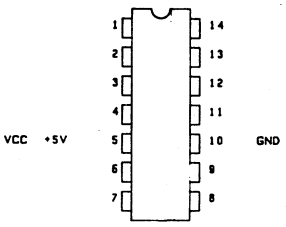
THIS DEVICE IS A 16 LINE TO 1 LINE DATA SELECTOR/MULTIPLEXER WITH STROBE. WHEN THE STROBE LINE IS LOW, DATA IS TRANSFERRED FROM THE INPUT SELECTED BY THE DATA SELECT LINES TO THE OUTPUT (NOTE THAT THE OUTPUT IS THE COMPLIMENT OF THE INPUT).

ELEMENT IDENTIFICATION #531
VENDOR IDENTIFICATION #74150

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 48	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

	OUTPUT			
COUNT	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

1. OUTPUT A CONNECTED TO INPUT B.
2. TO RESET ALL OUTPUTS TO LOGICAL 0 BOTH $R_{0(1)}$ AND $R_{0(2)}$ INPUTS MUST BE AT LOGICAL 1.
3. EITHER (OR BOTH) RESET INPUTS $R_{0(1)}$ AND $R_{0(2)}$ MUST BE AT A LOGICAL 0 TO COUNT.

TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A HIGH SPEED MONOLITTHIC 4 BIT BINARY COUNTER CONSISTING OF FOUR MASTER-SLAVE FLIP-FLOPS WHICH ARE INTERNALLY INTERCONNECTED TO PROVIDE A DIVIDE BY TWO COUNTER AND A DIVIDE BY EIGHT COUNTER.

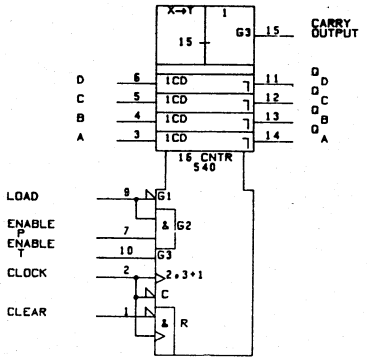
A GATED DIRECT RESET LINE IS PROVIDED WHICH INHIBITS THE COUNT INPUTS AND SIMULTANEOUSLY RETURNS FOUR FLIP-FLOP OUTPUTS TO A LOGICAL 0, AS THE OUTPUT FROM FLIP-FLOP A IS NOT INTERNALLY CONNECTED TO THE SUCCEEDING FLIP-FLOPS THE COUNTER MAY BE OPERATED IN TWO INDEPENDENT MODES

1. WHEN USED AS A 4-BIT RIPPLE-THROUGH COUNTER, OUTPUT A MUST BE EXTERNALLY CONNECTED TO INPUT B. THE INPUT COUNT PULSES ARE APPLIED TO INPUT A. SIMULTANEOUS DIVISIONS OF 2,4,8,16 ARE PREFORMED AT THE A,B,C,D OUTPUTS AS SHOWN IN THE TRUTH TABLE

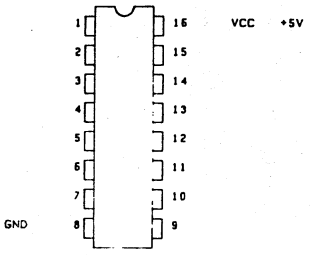
2. WHEN USED AS A 3 BIT RIPPLE-THROUGH COUNTER, THE INPUT COUNT PULSES ARE APPLIED TO INPUT B. SIMULTANEOUS FREQUENCY DIVISIONS OF 2, 4, AND 8 ARE AVAILABLE AT THE B,C,D OUTPUTS. INDEPENDENT USE OF FLIP-FLOP A IS AVAILABLE IF THE RESET FUNCTION COINCIDES WITH RESET OF THE 3-BIT RIPPLE-THROUGH COUNTER.

ELEMENT IDENTIFICATION #537
VENDOR IDENTIFICATION #7493

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)

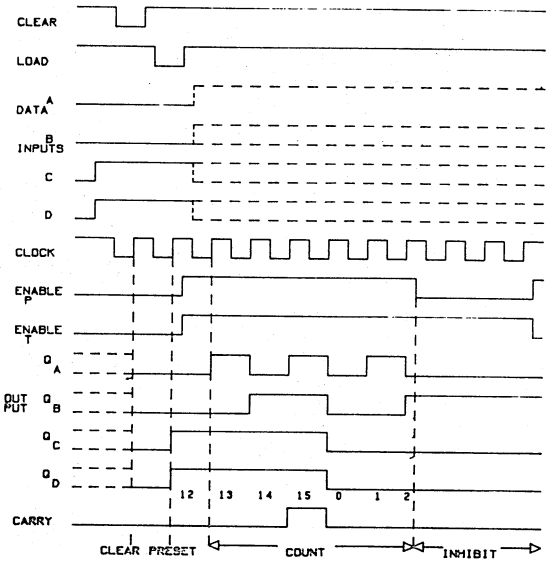


REV A
DWG NO C 95387500
SHEET 47
CODE IDENT
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC SEE DESCRIPTION

TIMING DIAGRAM
TYPICAL SEQUENCE OF OPERATION

1. CLEAR OUTPUT TO ZERO
2. PRESET TO BINARY TWELVE
3. COUNT TO THIRTEEN, FOURTEEN, FIFTEEN, ZERO, ONE, AND TWO
4. INHIBIT.

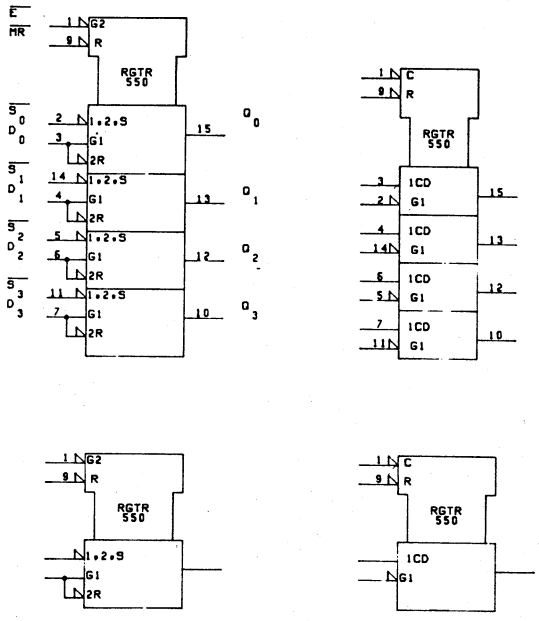


GENERAL OPERATIONAL DESCRIPTION

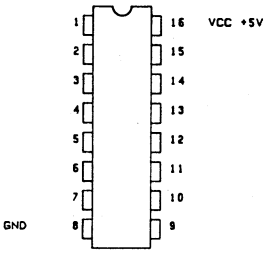
THIS 4-BIT BINARY COUNTER IS A SYNCHRONOUS, PRESETTABLE COUNTER WITH AN INTERNAL CARRY LOOK-AHEAD FOR APPLICATION IN HIGH-SPEED COUNTING SCHEMES. SYNCHRONOUS OPERATION IS PROVIDED BY HAVING ALL FLIP-FLOPS CLOCKED SIMULTANEOUSLY SO THAT THE OUTPUTS CHANGE COINCIDENT WITH EACH OTHER WHEN SO INSTRUCTED BY THE COUNT-ENABLE INPUTS AND INTERNAL GATING. THIS MODE OF OPERATION ELIMINATES THE OUTPUT COUNTING SPIKES WHICH ARE NORMALLY ASSOCIATED WITH ASYNCHRONOUS (RIPPLE CLOCK) COUNTERS. A BUFFERED CLOCK INPUT TRIGGERS THE FOUR J-K MASTER-SLAVE FLIP-FLOPS ON THE RISING (POSITIVE-GOING) EDGE OF THE CLOCK INPUT WAVEFORM. THIS COUNTER IS FULLY PROGRAMMABLE; THAT IS, THE OUTPUTS MAY BE PRESET TO EITHER STATE. AS PRESETTING IS SYNCHRONOUS, PLACING A LOW LEVEL ON THE LOAD INPUT DISABLES THE COUNTER AND CAUSES THE OUTPUTS TO AGREE WITH THE DATA INPUTS AFTER THE NEXT CLOCK PULSE. THE CLEAR FUNCTION IS SYNCHRONOUS AND A LOW LEVEL AT THE CLEAR INPUT SETS ALL FOUR OF THE FLIP-FLOP OUTPUT LOW AFTER THE NEXT CLOCK PULSE THIS SYNCHRONOUS CLEAR ALLOWS THE COUNT LENGTH TO BE MODIFIED EASILY AS DECODING THE MAXIMUM COUNT DESIRED CAN BE ACCOMPLISHED WITH ONE EXTERNAL NAND GATE. THE GATE OUTPUT IS CONNECTED TO THE CLEAR INPUT TO SYNCHRONOUSLY SET THE COUNTER TO 0000 (LLLL)
THE CARRY LOOK AHEAD CIRCUITRY PROVIDES FOR CASCADING COUNTERS FOR N-BIT SYNCHRONOUS APPLICATIONS WITHOUT ADDITIONAL GATING.
INPUT CLOCK FREQUENCY IS A MAXIMUM OF 25 MEGAHERTZ.

ELEMENT IDENTIFICATION #540
VENDOR IDENTIFICATION #74163

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS

REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	48

TRUTH TABLE
POS-LOGIC

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_N	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{N-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{N-1}	
H	H	X	X	Q_{N-1}	
L	X	X	X	L	RESET

1. X=IRRELEVANT
2. L=LOW VOLTAGE LEVEL =0
3. H=HIGH VOLTAGE LEVEL=1
4. Q_{N-1} =PREVIOUS OUTPUT STATE
5. Q_N =PRESENT OUTPUT STATE

TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE CONSISTS OF FOUR LATCHES WITH A COMMON ACTIVE LOW ENABLE AND AN ACTIVE LOW MASTER RESET. WHEN THE COMMON ENABLE GOES HIGH DATA PRESENT IN THE LATCH IS STORED AND THE STATE OF A LATCH IS NO LONGER AFFECTED BY THE $\overline{S}$ AND D INPUTS. THE MASTER RESET WHEN ACTIVATED OVERRIDES ALL OTHER INPUT CONDITIONS FORCING ALL LATCH OUTPUTS TO LOW. EACH OF THE FOUR LATCHES CAN BE OPERATED IN ONE OF TWO MODES.

D TYPE LATCH

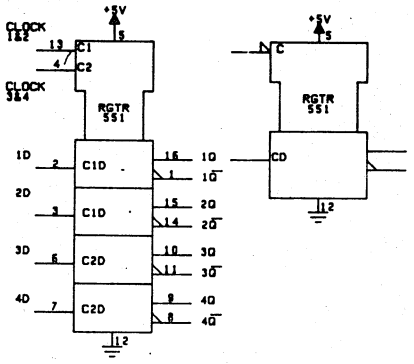
FOR D TYPE OPERATION THE $\overline{S}$ INPUT OF A LATCH IS HELD LOW. WHILE THE COMMON ENABLE IS ACTIVE THE LATCH OUTPUT FOLLOWS THE D INPUT. INFORMATION PRESENT AT THE LATCH OUTPUT IS STORED IN THE LATCH WHEN THE ENABLE GOES HIGH.

SET/RESET

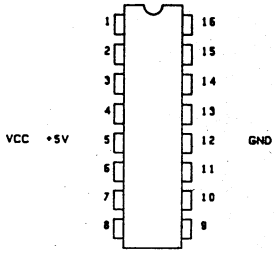
DURING SET/RESET OPERATION, WHEN THE COMMON ENABLE IS LOW A LATCH IS RESET BY A LOW ON THE D INPUT AND CAN BE SET BY A LOW ON THE $\overline{S}$ INPUT IF THE D INPUT IS HIGH. IF BOTH $\overline{S}$ AND D INPUTS ARE LOW THE D INPUT WILL DOMINATE AND THE LATCH WILL BE RESET. WHEN THE ENABLE GOES HIGH THE LATCH REMAINS IN THE LAST STATE PRIOR TO THE LOW TO HIGH TRANSITION.

ELEMENT IDENTIFICATION #550
VENDOR IDENTIFICATION #9314

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 40	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

T_N	T_{N+1}
1D	1Q
1	1
0	0

T_N = BIT TIME BEFORE CLOCK NEGATIVE-GOING TRANSITION

T_{N+1} = BIT TIME AFTER CLOCK NEGATIVE-GOING TRANSITION

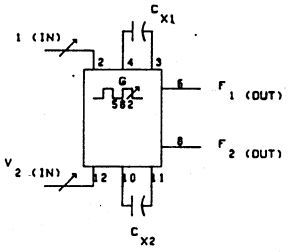
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A 4-BIT D-TYPE LATCH WITH COMPLEMENTARY Q AND $\overline{Q}$ OUTPUTS. INFORMATION PRESENT AT A DATA (D) INPUT IS TRANSFERRED TO THE Q OUTPUT WHEN THE CLOCK IS HIGH, AND THE Q OUTPUT WILL FOLLOW THE DATA INPUT AS LONG AS THE CLOCK REMAINS HIGH. WHEN THE CLOCK GOES LOW, THE INFORMATION (THAT WAS PRESENT AT THE DATA INPUT AT THE TIME THE TRANSITION OCCURED) IS RETAINED AT THE Q OUTPUT UNTIL THE CLOCK IS PERMITTED TO GO HIGH AGAIN.

TIMING DIAGRAM

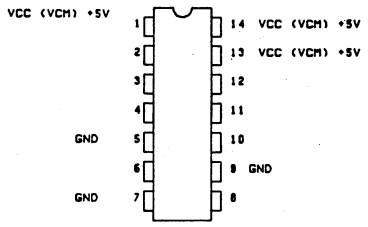
ELEMENT IDENTIFICATION #551
VENDOR IDENTIFICATION #7475

SYMBOL/APPLICATION/PINS



NOTE-- CX_1 AND CX_2 ARE EXTERNAL COMPONENTS

MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO 95387500
CODE IDENT C
SHEET 58

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

GENERAL OPERATIONAL DESCRIPTION

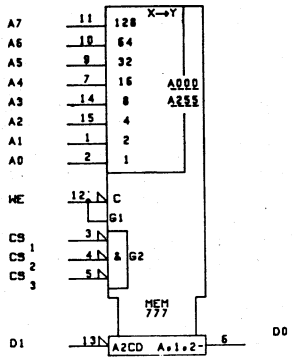
THIS DEVICE CONSISTS OF TWO INDEPENDENT VOLTAGE-CONTROLLED MULTIVIBRATORS WITH OUTPUT BUFFERS. VARIATION OF THE OUTPUT FREQUENCY OVER A 3.5-TO-1 RANGE IS GUARANTEED WITH AN INPUT DC CONTROL VOLTAGE OF 1.0 TO 5.0 VOLTAGE.

THE OPERATING FREQUENCY RANGE OF THIS MULTIVIBRATOR IS CONTROLLED BY THE VALUE OF THE EXTERNAL CAPACITOR CX_1 OR CX_2 AND, THE DC VOLTAGE INPUT CONTROL V1 OR V2. THIS DEVICES OUTPUT FREQUENCY IS CONTROLLED BY CX_1 , CX_2 AND THE INPUT VOLTAGE LOAD.

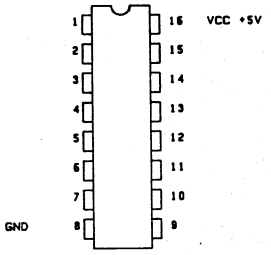
TIMING DIAGRAM

ELEMENT IDENTIFICATION #582
VENDOR IDENTIFICATION #MC4024

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO C 9538750 0
SHEET 51
CODE IDENT
KEY TO LOGIC SYMBOLS

TRUTH TABLE

CHIP SELECTS	WRITE ENABLE	OPERATION	OUTPUT
ALL 0	0	WRITE	LOGICAL 1 STATE
ALL 0	1	READ	COMPLIMENTARY OF DATA WRITTEN IN MEMORY
ONE OR MORE 1	X	HOLD	HIGH RESISTANCE STATE

TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

THIS INTEGRATED CIRCUIT IS A HIGH-SPEED, FULLY DECODED, STATIC BIPOLAR 256-BIT RANDOM ACCESS MEMORY IN A 256 WORD X 1 ORGANIZATION. THIS DEVICE FEATURES ON CHIP ADDRESS DECODING, THREE CHIP SELECTS,AND UNCOMMITTED COLLECTOR OUTPUTS.

READ OPERATION

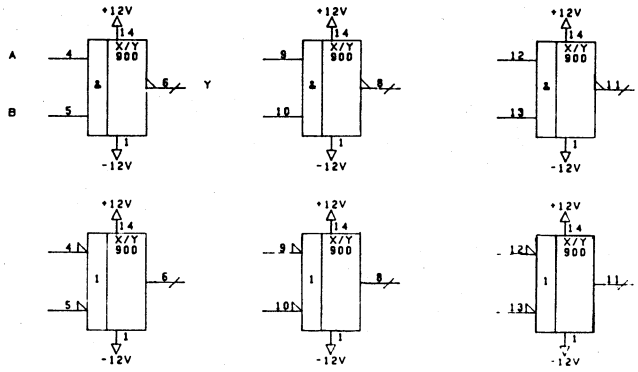
THE MEMORY IS ADDRESSED THROUGH THE A0-A7 INPUTS WHICH SELECT ONE OF THE 256 WORDS. THE CHIP IS ENABLED BY PLACING ALL CHIP SELECTS (CS) TO LOGIC 0. IF ANY OR ALL CS INPUTS ARE LOGICAL 1 THEN THE DEVICE WILL BE DISABLED. IF THE WRITE ENABLE (WE) IS AT LOGIC 1 THE STORED BIT IS READ OUT OF D0.

WRITE OPERATION

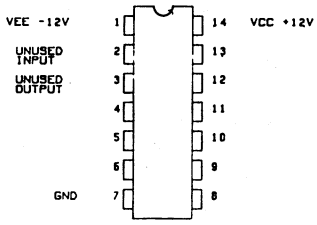
THE MEMORY IS ADDRESSED THROUGH THE A0-A7 INPUTS WHICH SELECT ONE OF THE 256 WORDS. THE CHIP IS ENABLED BY PLACING ALL THE CS INPUTS TO LOGICAL 0. IF THE WE INPUT IS AT A LOGICAL 0, THE DATA ON TERMINAL D1 IS WRITTEN INTO THE ADDRESSED WORD. WHEN WE RETURNS TO LOGIC 1, THE INFORMATION THAT WAS WRITTEN IN IS NOW READOUT. HOWEVER, EACH WORD READOUT IS THE COMPLEMENT OF WHAT WAS WRITTEN IN.

ELEMENT IDENTIFICATION #777
VENDOR IDENTIFICATION #74206

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A		
DWG NO	9538750 0		
CODE IDENT	C	SHEET 51A	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC Y=AB

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

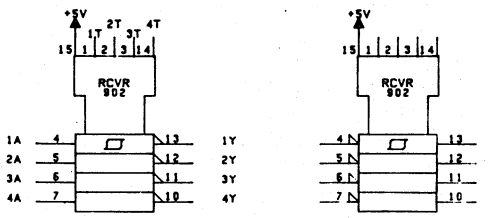
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A MONOLITHIC QUAD POS NAND LINE DRIVER COMPRISED OF THREE DUAL INPUT GATES AND ONE SINGLE INPUT GATE.

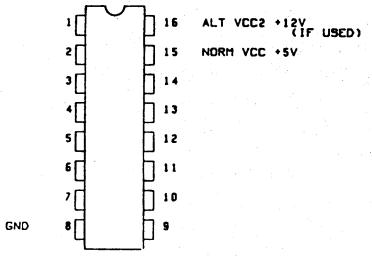
TIMING DIAGRAM

ELEMENT IDENTIFICATION #900
VENDOR IDENTIFICATION #MC1488L

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET 518

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS-LOGIC $Y = \overline{A}$

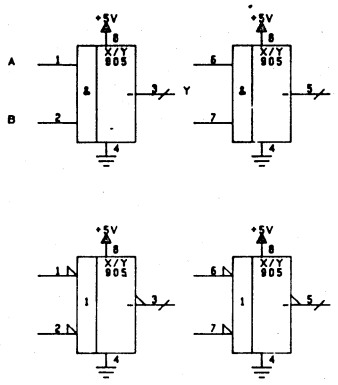
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

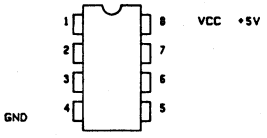
THIS DEVICE IS A MONOLITHIC QUADRUPLE LINE RECIEVER DESIGNED TO INTERFACE DATA TERMINAL EQUIPMENT WITH COMMUNICATIONS EQUIPMENT. OTHER APPLICATIONS ARE FOR POINT TO POINT DATA TRANSMISSION AND FOR LEVEL TRANSLATORS. OPERATION IS NORMALLY FROM A SINGLE 5 VOLT SUPPLY, HOWEVER A BUILT IN OPTION ALLOWS OPERATION FROM A 12 VOLT SUPPLY WITHOUT THE USE OF ADDITIONAL COMPONENTS.
IN NORMAL OPERATION, THE THRESHOLD CONTROL TERMINALS (1T, 2T, 3T, AND 4T) ARE CONNECTED TO THE VCC1 TERMINAL PIN 15 EVEN IF POWER IS BEING SUPPLIED VIA THE ALTERNATE VCC2 TERMINAL, PIN 16. IN THIS MODE OF OPERATION, IF THE INPUT VOLTAGE GOES TO ZERO, THE OUTPUT VOLTAGE WILL REMAIN AT THE LOW OR HIGH LEVEL AS DETERMINED BY THE PREVIOUS INPUT.
FOR FAILSAFE OPERATION, THE THRESHOLD-CONTROL TERMINALS ARE OPEN. IN THIS MODE OF OPERATION, IF THE INPUT VOLTAGE GOES TO ZERO OR AN OPEN CIRCUIT CONDITION, THE OUTPUT WILL GO TO THE HIGH LEVEL REGARDLESS OF THE PREVIOUS INPUT CONDITION.

ELEMENT IDENTIFICATION #902
VENDOR IDENTIFICATION #75154

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	S2

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS-LOGIC Y=AB

A	B	Y	
0	0	0	ON STATE
0	1	0	ON STATE
1	0	0	ON STATE
1	1	1	OFF STATE

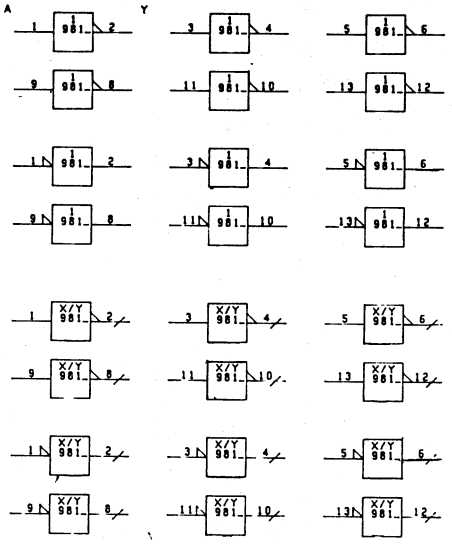
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL PERIPHERAL POSITIVE AND DRIVER (ASSUMING POSITIVE LOGIC) WITH THE OUTPUT OF THE LOGIC GATES INTERNALLY CONNECTED TO THE BASES OF THE N-P-N OUTPUT TRANSISTORS. THE CIRCUIT OUTPUTS ARE OPEN COLLECTOR OUTPUTS.

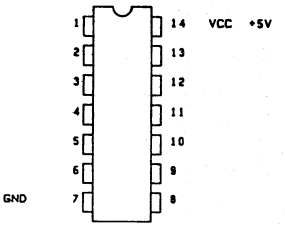
TIMING DIAGRAM

ELEMENT IDENTIFICATION #805
VENDOR IDENTIFICATION #75451

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE
POS LOGIC $Y=\overline{A}$

A	Y
0	1
1	0

GENERAL OPERATIONAL DESCRIPTION

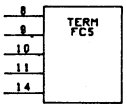
THIS DEVICE IS A HEX INVERTER BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS.

TIMING DIAGRAM

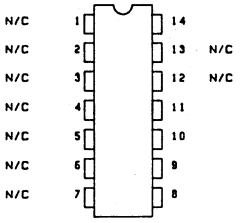
ELEMENT IDENTIFICATION #981
VENDOR IDENTIFICATION #7416

REV A
DWG NO C 95387500
SHEET 53
CODE IDENT
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO C 95387500
SHEET 54
CODE IDENT

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

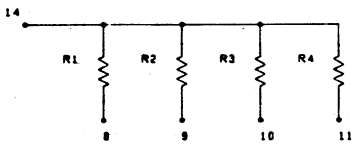
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE CONTAINS FOUR RESISTORS WITH THE INDICATED VALUES.

COMPONENT	VALUE
R1	20 OHMS
R2	20 OHMS
R3	20 OHMS
R4	20 OHMS

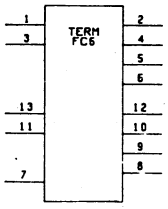
THIS DEVICE IS DESIGNED FOR USE IN CONJUNCTION WITH THE DRVR DEVICE.

CIRCUIT DIAGRAM

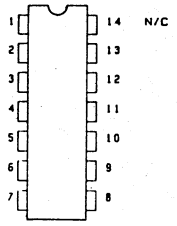


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # FC5

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	9538750O
CODE IDENT	C
SHEET	55

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

GENERAL OPERATIONAL DESCRIPTION

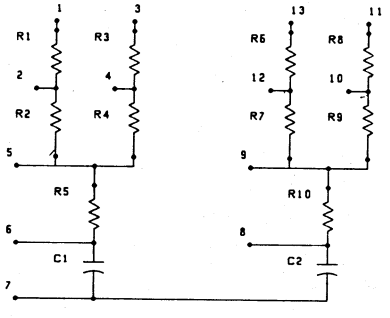
THIS DEVICE CONTAINS 10 RESISTORS AND 2 NON-POLARIZED CAPACITORS WITH THE INDICATED VALUES.

COMPONENT	VALUE
R1	33 OHMS
R2	22 OHMS
R3	33 OHMS
R4	22 OHMS
R5	15 OHMS
R6	33 OHMS
R7	22 OHMS
R8	33 OHMS
R9	22 OHMS
R10	15 OHMS
C1	.1MFD
C2	.1MFD

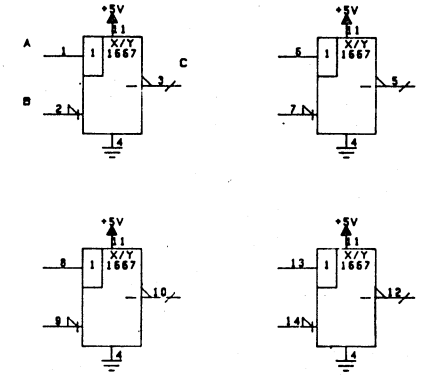
THIS DEVICE IS DESIGNED FOR USE IN CONJUNCTION WITH THE RCVR DEVICE.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # FC6

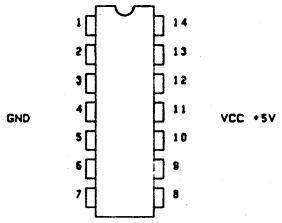
CIRCUIT DIAGRAM



SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
DWG NO	95387500	
CODE IDENT	C	SHEET 56

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $C=\overline{AB}$

A	B	C
1	1	0
0	1	1
1	0	1
0	0	1

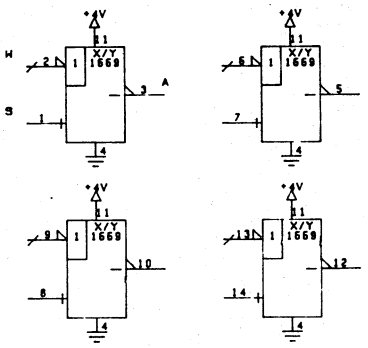
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A MONOLITHIC QUAD TWO INPUT NAND GATE CAPABLE OF DRIVING 8 NORMALIZED LOADS.

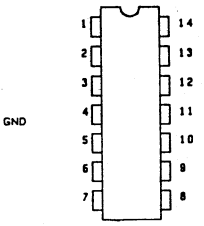
TIMING DIAGRAMS

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #1667

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



GND

VCC +4V

REV	A		
DWG NO	95387500		
CODE IDENT	C	SHEET 57	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

S	H	A
1	1	1
1	0	1
0	1	1
0	0	0

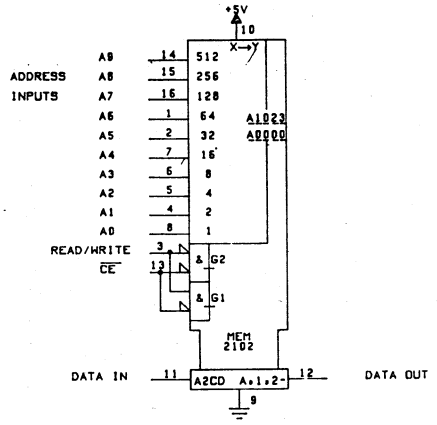
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A MONOLITHIC QUAD TWO INPUT AMPLIFIER. CAPABLE OF DRIVING 8 NORMALIZED LOADS.

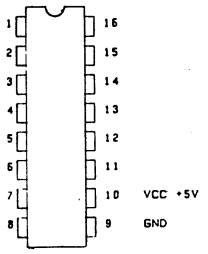
TIMING DIAGRAM

ELEMENT IDENTIFICATION
VENDOR IDENTIFICATION # 1669

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 57A	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

CHIP ENABLE	READ/ WRITE	OPERATION	OUTPUT
0	0	WRITE	LOGICAL 1 STATE
0	1	READ	LOGICAL 1 STATE
1	X	HOLD	HIGH RESISTANCE STATE

X = IRRELEVENT

TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A HIGH-SPEED, FULLY DECODED, MONOLITHIC 1024-BIT RANDOM ACCESS MEMORY IN A 1024 WORD BY 1 ORGANIZATION. THIS DEVICE FEATUES ON CHIP ADDRESS DECODING, ONE CHIP SELECT, ONE READ-WRITE ENABLE AND TRI-STATE OUTPUT CAPABILITY.

READ OPERATION

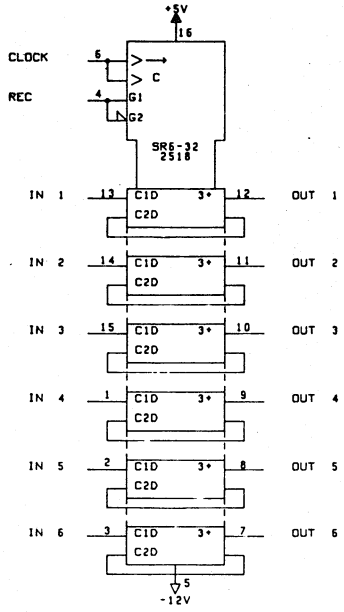
THE MEMORY IS ADDRESSED THROUGH THE A0-A9 INPUTS WHICH SELECT ONE OF THE 1024 WORDS. THE CHIP IS ENABLED BY PLACING THE CHIP ENABLE TO LOGICAL 0. IF THE READ-WRITE ENABLE IS AT A LOGICAL 1, THE STORED BIT IS READ OUT OF DATA OUT.

WRITE OPERATION

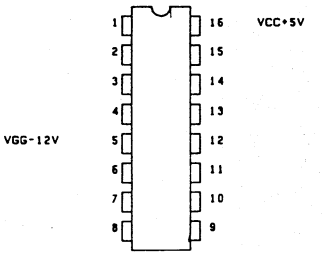
THE MEMORY IS ADDRESSED THROUGH THE A0-A9 INPUTS, WHICH SELECT ONE OF THE 1024 WORDS. THE CHIP IS ENABLED BY PLACING THE CHIP ENABLE AT A LOGICAL 0. IF THE READ-WRITE ENABLE IS AT A LOGICAL 0, THE DATA ON TERMINAL DATA-IN IS WRITTEN INTO THE ADDRESSED WORD WHEN READ-WRITE ENABLE RETURNS TO A LOGICAL 1. THE INFORMATION THAT WAS WRITTEN IS NOW READ OUT.

ELEMENT IDENTIFICATION #772
VENDOR IDENTIFICATION #2102

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A		
DWG NO	C	95387500	SHEET 5B
CODE IDENT			

KEY TO LOGIC SYMBOLS

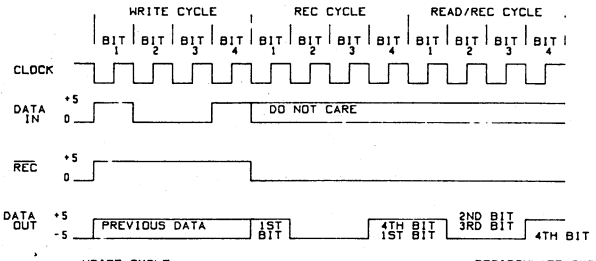
TRUTH TABLE
POS-LOGIC

RECIRCULATE	INPUT	FUNCTION
1	0	RECIRCULATE
1	1	RECIRCULATE
0	0	0 IS WRITTEN
0	1	1 IS WRITTEN

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A HEX 32 BIT RECIRCULATING STATIC SHIFT REGISTER FEATURING SINGLE ENDED (BARE DRAIN) BUFFERS. NO OUTPUT LOAD IMPEDANCE. IT CONSISTS OF SIX SECTIONS WITH COMMON CLOCK AND RECIRCULATE CONTROL.

TIMING DIAGRAM-(TYPICAL 4 BIT SEQUENCE)



WRITE CYCLE

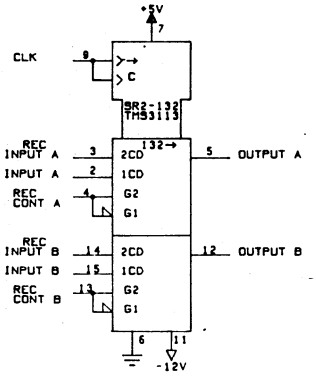
THE POSITIVE EDGE OF THE REC CONTROL IS COINCIDENT WITH THE NEG GOING CLOCK EDGE. THE OUTPUT ENABLE CONTROL MAY BE 1 OR 0 IF=1 PREVIOUS DATA WILL BE READ AND THE 1ST BIT WILL BE READ AFTER THE FOURTH RISING CLOCK EDGE.

RECIRCULATE CYCLE

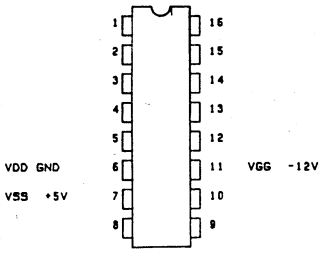
DATA RECIRCULATES WHILE THE RECIRCULATE CONTROL IS 0 NEW INPUT DATA IS IGNORED. OUTPUT DATA IS READ OUT DURING THIS TIME.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #2518

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO 95387500
CODE IDENT C
SHEET 58

KEY TO LOGIC SYMBOLS

GENERAL OPERATIONAL DESCRIPTION

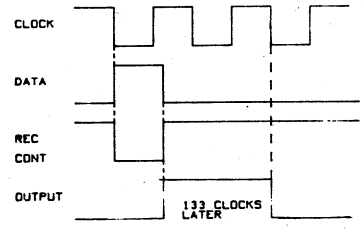
THE TMS 3113 JC/NC IS A STATIC ACCUMULATOR CONSISTING OF TWO SEPERATE STATIC SHIFT REGISTERS WITH INDEPENDENT INPUT AND OUTPUT TERMINALS AND LOGIC FOR LOADING OR RECIRCULATING INFORMATION. THE TWO SHIFT REGISTERS ARE 133 BIT DEVICES.

A SINGLE CLOCK IS REQUIRED FOR OPERATION. THE CLOCK AND ALL INPUTS CAN BE DRIVEN DIRECTLY FROM DTL/TTL LOGIC LEVELS AND EACH REGISTER OUTPUT CAN DRIVE DTL/TTL CIRCUITS. THREE CLOCKS ARE GENERATED INTERNALLY. CROSS-COUPLED FLIP-FLOPS ARE USED TO IMPLEMENT EACH BIT OF DELAY AND ENABLE DATA TO BE STORED INDEFINITELY BETWEEN CLOCK PULSES. THIS DEVICE IS CAPABLE OF OPERATION FROM DC TO 2 MEGAHERTZ.

TRANSFERRING DATA INTO THE REGISTER IS ACCOMPLISHED WHEN THE CLOCK AND RECIRCULATE CONTROL ARE AT LOGIC 0. FOR LONG-TERM DATA STORAGE THE CLOCK MUST BE HELD AT A LOGIC 1. RECIRCULATE OCCURS WHEN THE RECIRCULATE CONTROL IS A LOGIC 1. OUTPUT DATA APPEARS ON THE 0-TO-1 TRANSITION OF THE CLOCK PULSE.

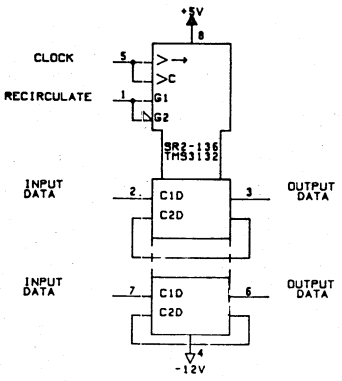
TRUTH TABLE
POS-LOGIC

TIMING DIAGRAM

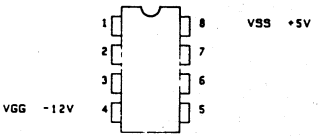


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #TMS 3113

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO C 95387500

SHEET 60

CODE IDENT

KEY TO LOGIC SYMBOLS

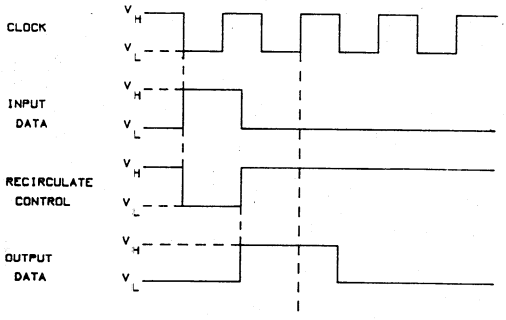
TRUTH TABLE
POS LOGIC

GENERAL OPERATIONAL DESCRIPTION

DATA IS TRANSFERRED INTO THE SHIFT REGISTER WHILE THE RECIRCULATE CONTROL IS AT A LOGIC HIGH LEVEL. OUTPUT DATA IS AVAILABLE IN THE RECIRCULATE MODE. RECIRCULATE OCCURS WHEN RECIRCULATE CONTROL IS AT A LOW LEVEL.

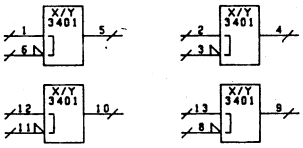
TRANSFER OF DATA INTO THE SHIFT REGISTER IS COMPLETED ON THE LOW-TO-HIGH TRANSITION OF THE CLOCK. DATA IS EXTRACTED FROM THE SHIFT REGISTER ON THE LOW-TO-HIGH TRANSITION OF RECIRCULATE. FOR LONG-TERM DATA STORAGE, THE CLOCK MUST BE MAINTAINED AT A LOGIC HIGH. MAXIMUM SPEED OF OPERATION IS 2.5 MEGAHERTZ

TIMING DIAGRAM

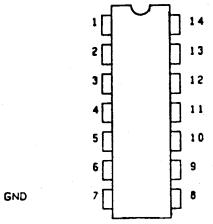


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #TMS 3132

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO 95387500
SHEET 61
CODE IDENT C
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

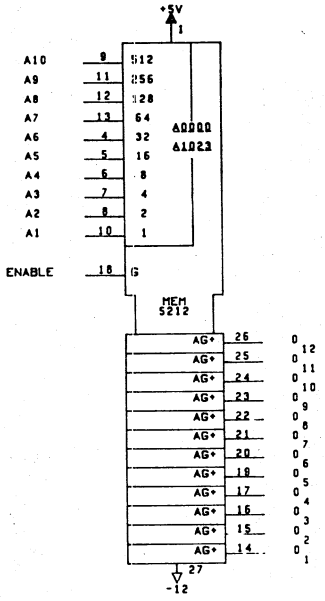
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE CONTAINS FOUR INDEPENDENT OPERATIONAL AMPLIFIERS THAT ARE INTERNALLY COMPENSATED FOR SINGLE POSITIVE POWER SUPPLY APPLICATIONS. LOW LEVEL DIFFERENTIAL INPUTS ARE CONVERTED TO SINGLE-ENDED HIGH LEVEL OUTPUTS.

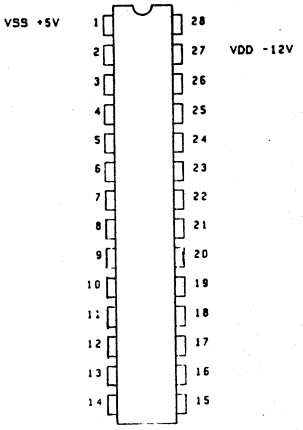
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #3401

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO C 95387500

SHEET 62

CODE IDENT

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

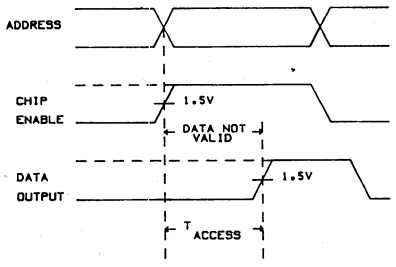
GENERAL OPERATIONAL DESCRIPTION

THIS INTEGRATED CIRCUIT IS A HIGH-SPEED FULLY DECODED MOS 12,228-BIT READ ONLY MEMORY IN A 1024 WORD X 12 ORGANIZATION. THIS DEVICE FEATURES ON CHIP ADDRESS DECODING, ONE CHIP ENABLE, AND OPEN DRAIN OUTPUT. (NO OUTPUT LOAD IMPEDANCE).

READ OPERATION

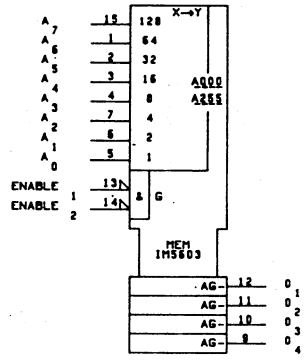
THE MEMORY IS ADDRESSED THROUGH THE A1-A10 INPUTS WHICH SELECTS ONE OF THE 1024 WORDS. THE CHIP IS ENABLED BY PLACING THE CHIP ENABLE TO A LOGICAL 1. WHEN THE ENABLE = LOGICAL 0, THEN THE DEVICE IS DISABLED, AND THE OUTPUT ARE IN THE LOW STATE.

TIMING DIAGRAM

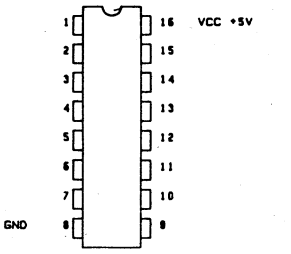


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #MM5212

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

CODE IDENT C

DWG NO 95387500

SHEET 03

KEY TO LOGIC SYMBOLS

TRUTH TABLE

MEMORY READING

TO READ THE MEMORY, BOTH CHIP ENABLE INPUTS ARE HELD LOW. THE OUTPUTS THEN CORRESPOND TO THE DATA PROGRAMMED IN THE SELECTED WORD. WITH EITHER OR BOTH OF THE CHIP ENABLE INPUTS HIGH, ALL OUTPUTS ARE FLOATING.

TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A HIGH SPEED ELECTRICALLY PROGRAMMABLE FULLY DECODED TTL BIPOLAR 1024 BIT ''READ ONLY'' MEMORIES ORGANIZED AS 256 WORDS BY 4 BITS. THE DEVICE ALSO PROVIDES ON CHIP ADDRESS DECODING TWO CHIP ENABLE INPUTS AND UNCOMMITTED COLLECTOR OUTPUTS, WHICH ALLOW SIMPLIFIED MEMORY EXPANSION. THIS MEMORY IS FABRICATED WITH ALL LOGIC LEVEL ZEROS (LOW). LOGIC LEVEL ONES (HIGH) CAN BE ELECTRICALLY PROGRAMMED IN SELECTED BIT LOCATIONS. THE SAME ADDRESS INPUTS ARE USED FOR BOTH PROGRAMMING AND READING.

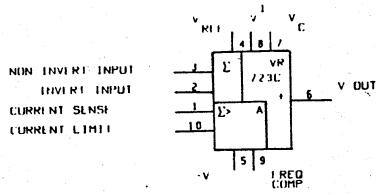
PROGRAMMING

A LOGIC ONE CAN BE PERMANENTLY PROGRAMMED INTO A SELECTED BIT LOCATION USING SPECIAL EQUIPMENT.

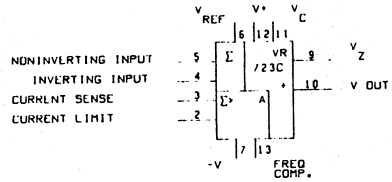
ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION #IM5603

SYMBOL/APPLICATION PINS

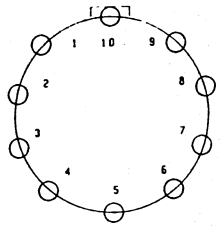


10 LEAD METAL CAN SYMBOL



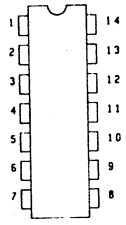
14 PIN DIP SYMBOL

MECHANICAL CONFIGURATION (TOP VIEW)
(TO100)



NOTE-- PIN 5 IS CONNECTED TO THE CASE

MECHANICAL CONFIGURATION (TOP VIEW)
(TO116)



REV E
DWG NO 9538750
SHEET 64
CODE IDENT C
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A VOLTAGE REGULATOR DESIGNED PRIMARILY FOR SERIES REGULATOR APPLICATIONS. BY ITSELF, IT WILL SUPPLY OUTPUT CURRENTS UP TO 150MA. BUT EXTERNAL TRANSISTORS CAN BE ADDED TO PROVIDE ANY DESIRED LOAD CURRENT. THE CIRCUIT FEATURES LOW STANDBY CURRENT DRAIN, AND PROVISION IS MADE FOR EITHER LINEAR OR FOLDBACK CURRENT LIMITING.

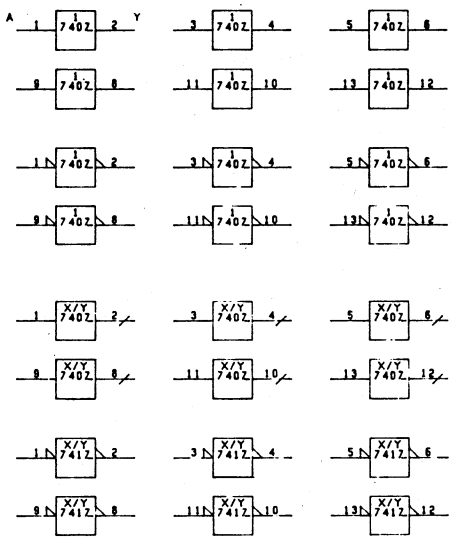
CHARACTERISTICS ARE

1. 150MA OUTPUT CURRENT WITHOUT EXTERNAL PASS TRANSISTOR
2. OUTPUT CURRENTS IN EXCESS OF 10A POSSIBLE BY ADDING EXTERNAL TRANSISTORS.
3. MAX INPUT VOLTAGE = 40 VOLTS
4. OUTPUT VOLTAGE ADJUSTABLE FROM 2VOLTS TO 37VOLTS
5. MAY BE USED AS EITHER A LINEAR OR A SWITCHING REGULATOR.

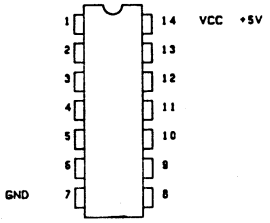
TIMING DIAGRAM

ELEMENT IDENTIFICATION # 334 (TO116 ONLY)
VENDOR IDENTIFICATION #723C (TO116 & TO100)

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



CODE IDENT	C	DWG NO 95387500	REV A
		SHEET 65	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC Y=A

A	Y
1	1
0	0

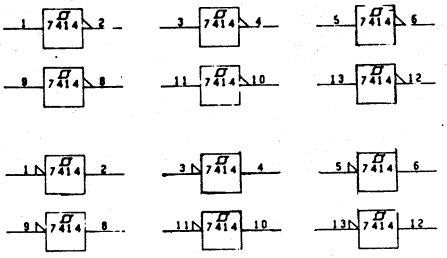
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TTL HEX BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS

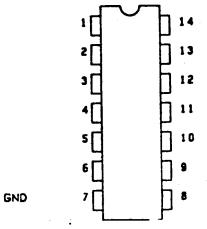
TIMING DIAGRAM

ELEMENT IDENTIFICATION #227
VENDOR IDENTIFICATION #7407

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 66	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC $Y=\overline{A}$

A	Y
1	0
0	1

GENERAL OPERATIONAL DESCRIPTION

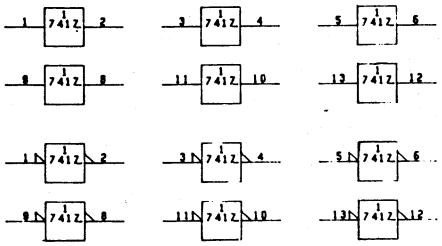
THIS DEVICE IS A TTL HEX-SCHMIDT TRIGGER POSITIVE INVERTER WITH TOTEM-POLE OUTPUTS.
POSITIVE THRESHOLD=1.5V
NEGATIVE THRESHOLD=1.1V

TIMING DIAGRAM

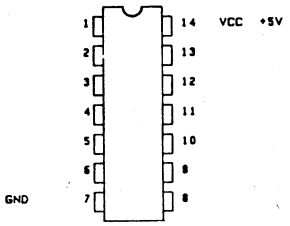
ELEMENT IDENTIFICATION #943
VENDOR IDENTIFICATION # 7414

SYMBOL/APPLICATION/PINS

A Y



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
SHEET 07	
CODE IDENT	C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC Y=A

A	Y
1	1
0	0

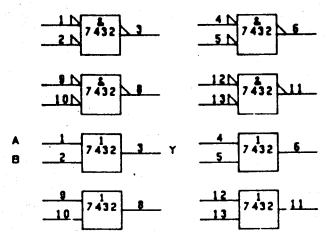
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TTL HEX BUFFER/DRIVER WITH OPEN COLLECTOR HIGH-VOLTAGE OUTPUTS.

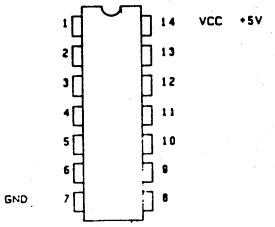
TIMING DIAGRAM

ELEMENT IDENTIFICATION 0868
VENDOR IDENTIFICATION 07417

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	C 95387500
CODE IDENT	SHEET 68

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC Y=A+B

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

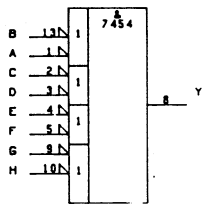
GENERAL OPERATIONAL DESCRIPTION

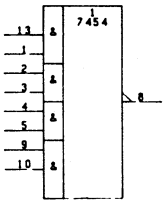
THIS DEVICE IS A QUADRUPLE 2 INPUT TTL POSITIVE OR GATE.

TIMING DIAGRAM

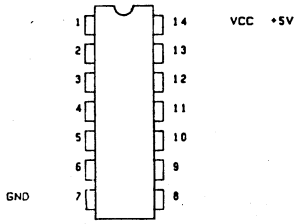
ELEMENT IDENTIFICATION #218
VENDOR IDENTIFICATION #7432

SYMBOL/APPLICATION/PINS





MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	68

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC $Y=(\overline{AB})+(CD)+(EF)+(GH)$

A	B	C	D	E	F	G	H	Y
0	X	0	X	0	X	0	X	1
X	0	X	0	X	0	X	0	1
1	1	X	X	X	X	X	X	0
X	X	1	1	X	X	X	X	0
X	X	X	X	1	1	X	X	0
X	X	X	X	X	X	1	1	0
ETCETRA								

X= IRRELEVANT

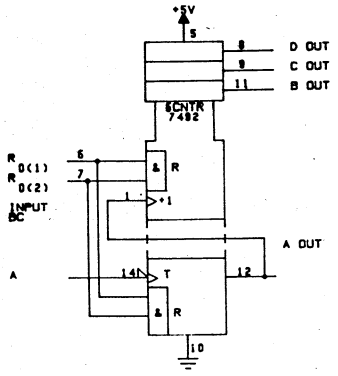
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A 4 WIDE 2-INPUT TTL AND-OR-INVERT GATE.

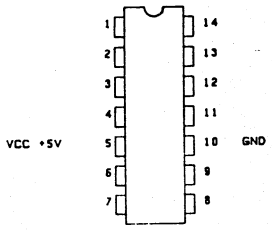
TIMING DIAGRAM

ELEMENT IDENTIFICATION
VENDOR IDENTIFICATION #7454

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
DWG NO	95387500	
CODE IDENT	C	SHEET 68A

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES

1. OUTPUT A CONNECTED TO INPUT B
2. TO RESET ALL OUTPUTS TO LOGICAL 0 BOTH $R_{0(1)}$ AND $R_{0(2)}$ INPUTS MUST BE AT LOGICAL 1
3. EITHER (OR) BOTH RESET INPUTS $R_{0(1)}$ AND $R_{0(2)}$ MUST BE AT A LOGICAL 0 COUNT

TIMING DIAGRAM

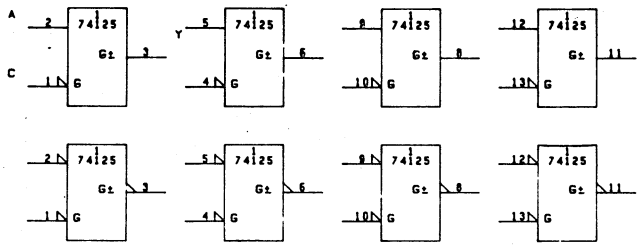
GENERAL OPERATIONAL DESCRIPTION

THIS HIGH SPEED MONOLITHIC 4 BIT BINARY COUNTER CONSISTS OF FOUR MASTER SLAVE FLIP-FLOPS WHICH ARE INTERNALLY CONNECTED TO PROVIDE A DIVIDE BY TWO COUNTER AND A DIVIDE BY 6 COUNTER. A GATED DIRECT RESET LINE IS PROVIDED WHICH INHIBITS THE COUNT INPUTS AND SIMULTANEOUSLY RETURNS THE FOUR FLIP-FLOP OUTPUTS TO A LOGICAL 0. AS THE OUTPUT FROM FLIP-FLOP A IS NOT INTERNALLY CONNECTED TO THE SUCCEEDING FLIP-FLOPS THE COUNTER MAY BE OPERATED IN TWO INDEPENDENT MODES

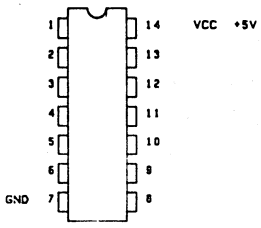
1. WHEN USED AS A DIVIDE-BY-TWELVE COUNTER, OUTPUT A MUST BE EXTERNALLY CONNECTED TO INPUT BC. THE INPUT COUNT PULSES ARE APPLIED TO INPUT A. SIMULTANEOUS DIVISIONS OF 2, 6, AND 12 ARE PERFORMED AT THE A, C, AND D OUTPUTS AS SHOWN IN THE TRUTH TABLE.
2. WHEN USED AS A DIVIDE-BY-SIX COUNTER, THE INPUT COUNT PULSES ARE APPLIED TO INPUT BC. SIMULTANEOUSLY, FREQUENCY DIVISIONS OF 3 AND 6 ARE AVAILABLE AT THE C AND D OUTPUTS. INDEPENDENT USE OF FLIP-FLOP A IS AVAILABLE IF THE RESET FUNCTION COINCIDES WITH RESET OF THE DIVIDE-BY-SIX COUNTER.

ELEMENT IDENTIFICATION #548
VENDOR IDENTIFICATION #7492

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
CODE IDENT	C	DWG NO 95387500 SHEET 78

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC Y=A
OUTPUT IS OFF (HIGH IMPEDANCE STATE)
WHEN C IS HIGH

A	C	Y
1	0	1
1	1	OFF
0	0	0
0	1	OFF

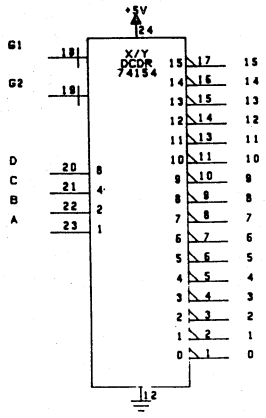
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE TTL BUSS BUFFER GATE WITH THREE-STATE OUTPUTS.

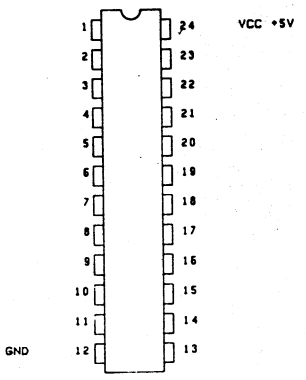
TIMING DIAGRAM

ELEMENT IDENTIFICATION #216
VENDOR IDENTIFICATION #74125

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET 71

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUT					OUTPUT														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

NOTES 1. H = HIGH
2. L = LOW
3. X = IRRELEVANT

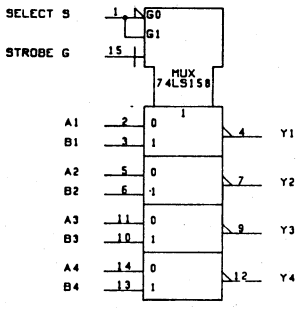
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

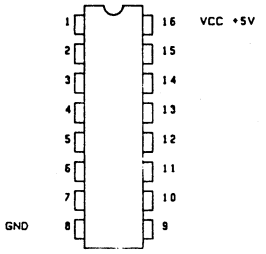
THIS MONOLITHIC 4-LINE-TO-16-LINE DECODER UTILIZES TTL CIRCUITRY TO DECODE FOUR BINARY-CODED INPUTS INTO ONE OF SIXTEEN MUTUALLY EXCLUSIVE OUTPUTS WHEN BOTH THE STROBE INPUTS G1 AND G2 ARE LOW. THE DEMULTIPLEXING FUNCTION IS PERFORMED BY USING THE 4 INPUT LINES TO ADDRESS THE OUTPUT LINE. PASSING DATA FROM ONE OF THE STROBE INPUTS WITH THE OTHER STROBE INPUT LOW. WHEN EITHER STROBE INPUT IS HIGH, ALL OUTPUTS ARE HIGH.

ELEMENT IDENTIFICATION #167
VENDOR IDENTIFICATION #74154

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

SHEET 72

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS-LOGIC

INPUTS				OUTPUTS
STROBE G	SELECT S	DATA A	DATA B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH

L = LOW

X = IRRELEVANT

GENERAL OPERATIONAL DESCRIPTION

THIS TTL DEVICE IS A QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR / MULTIPLEXER CONSISTING OF FOUR MULTIPLEXING CIRCUITS WITH COMMON SELECT AND ENABLE LOGIC. EACH CIRCUIT CONTAINS TWO INPUTS AND ONE OUTPUT.

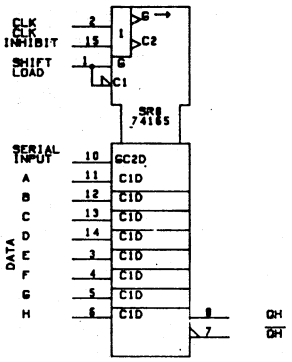
THIS DEVICE HAS THE ABILITY TO SELECT FOUR BITS OF DATA FROM EITHER OF TWO SOURCES AND WILL PRESENT INVERTED DATA (WITH RESPECT TO THE INPUTS) AT EACH OUTPUT. WITH A MINIMIZED PROPAGATION DELAY.

ELEMENT IDENTIFICATION #

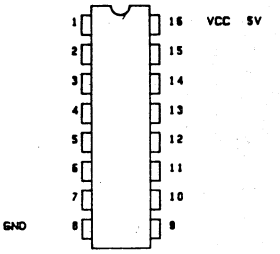
VENDOR IDENTIFICATION #74LS158

TIMING DIAGRAM

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO 95387500
CODE IDENT C
SHEET 73

KEY TO LOGIC SYMBOLS

TRUTH TABLE

POS-LOGIC SEE DESCRIPTION

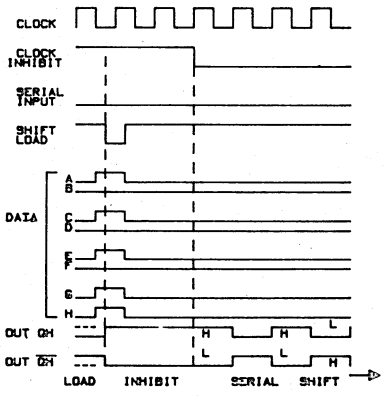
GENERAL OPERATIONAL DESCRIPTION

THE SN74165 IS AN 8 BIT SERIAL SHIFT REGISTER THAT SHIFTS THE DATA TO THE OUTPUT WHEN CLOCKED. PARALLEL-IN ACCESS TO EACH STAGE IS MADE AVAILABLE BY EIGHT INDIVIDUAL DIRECT DATA INPUTS WHICH ARE ENABLED BY A LOW LEVEL AT THE SHIFT/LOAD INPUT. THIS REGISTER ALSO HAS GATED CLOCK INPUTS AND COMPLEMENTARY OUTPUTS FROM THE EIGHTH BIT.

CLOCKING IS ACCOMPLISHED THROUGH A TWO INPUT POSITIVE-NOR GATE PERMITTING ONE INPUT TO BE USED AS A CLOCK-INHIBIT FUNCTION. HOLDING EITHER OF THE CLOCK INPUTS HIGH INHIBITS CLOCKING AND HOLDING EITHER CLOCK INPUT LOW WITH THE LOAD INPUT HIGH ENABLES THE OTHER CLOCK INPUT. THE CLOCK-INHIBIT INPUT SHOULD BE CHANGED TO THE HIGH ONLY WHILE THE CLOCK INPUT IS HIGH. PARALLEL LOADING IS INHIBITED AS LONG AS THE LOAD INPUT IS HIGH. WHEN TAKEN LOW, DATA AT THE PARALLEL INPUTS ARE LOADED DIRECTLY INTO THE REGISTER INDEPENDENTLY OF THE STATE OF THE CLOCK. MAXIMUM INPUT CLOCK FREQUENCY IS 20 MEGAHERTZ.

TIMING DIAGRAM

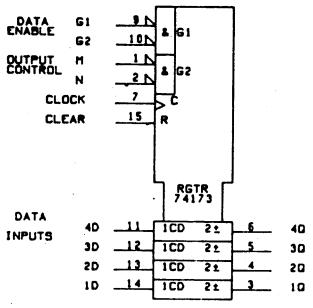
SHIFT-LOAD-INHIBIT SEQUENCE



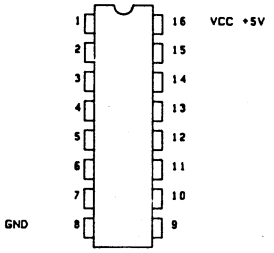
ELEMENT IDENTIFICATION #547

VENDOR IDENTIFICATION #74165

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 74	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUT					OUTPUT
CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

WHEN EITHER M OR N (OR BOTH) IS (ARE) HIGH THE OUTPUT IS DISABLED TO THE HIGH-IMPEDANCE STATE HOWEVER SEQUENTIAL OPERATION OF THE FLIP-FLOP IS NOT AFFECTED.

1. H=HIGH LEVEL (STEADY STATE)=1
2. L=LOW LEVEL (STEADY STATE)=0
3. ↑ =LOW-TO-HIGH-LEVEL TRANSITION
4. X=IRRELEVANT (ANY INPUT INCLUDING TRANSITION)
5. Q_0=THE LEVEL OF Q BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED.

TIMING DIAGRAM

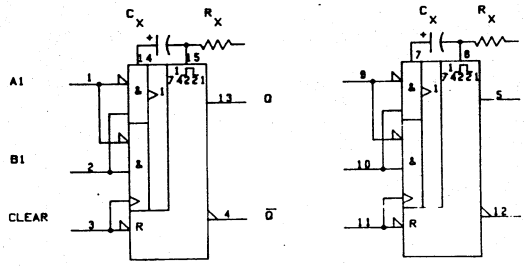
GENERAL OPERATIONAL DESCRIPTION

THIS 4-BIT REGISTER INCLUDES D-TYPE FLIP-FLOPS FEATURING TOTEM-POLE THREE-STATE OUTPUTS CAPABLE OF DRIVING HIGHLYCAPACITIVE OR RELATIVELY LOW-IMPEDANCE LOADS. THE HIGH-IMPEDANCE THIRD STATE AND INCREASED HIGH-LOGIC-LEVEL DRIVE PROVIDE THESE FLIP-FLOPS WITH THE CAPABILITY OF BEING CONNECTED DIRECTLY TO AND DRIVING THE BUS LINES IN A BUS-ORGANIZED SYSTEM WITHOUT NEED FOR INTERFACE OR PULL-UP COMPONENTS.

GATED ENABLE INPUTS ARE PROVIDED FOR CONTROLLING THE ENTRY OF DATA INTO THE FLIP-FLOPS. WHEN BOTH DATA-ENABLE INPUTS ARE LOW, DATA AT THE D INPUTS ARE LOADED INTO THEIR RESPECTIVE FLIP-FLOP ON THE NEXT POSITIVE TRANSITION OF THE BUFFERED CLOCK INPUT. GATE OUTPUT CONTROL INPUTS ARE ALSO PROVIDED. WHEN BOTH ARE LOW, THE NORMAL LOGIC STATES (HIGH OR LOW LEVEL) OF THE FOUR OUTPUTS ARE AVAILABLE FOR DRIVING THE LOADS OR BUS LINES. THE OUTPUTS ARE DISABLED INDEPENDENTLY FROM THE LEVEL OF THE CLOCK BY A HIGH LOGIC LEVEL AT EITHER OUTPUT CONTROL INPUT. THE OUTPUTS THEN PRESENT A HIGH IMPEDANCE AND NEITHER LOAD NOR DRIVE THE BUS LINE.

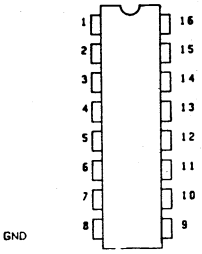
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #74173

SYMBOL/APPLICATIONS/PINS



NOTE C_X AND R_X ARE EXTERNAL COMPONENTS.

MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	9538750
CODE IDENT	C
SHEET 75	

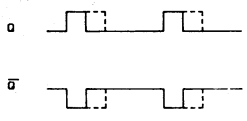
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUTS			OUTPUT	
CLR	A1	B1	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍

NOTES
1. H= HIGH LEVEL (STEADY STATE)
2. L= LOW LEVEL (STEADY STATE)
3. ↑ = TRANSITION FROM LOW TO HIGH
4. ↓ = TRANSITION FROM HIGH TO LOW
5. ⎍ = ONE HIGH-LEVEL PULSE
6. ⎎ = ONE LOW-LEVER PULSE
7. X= IRREVELANT
8. LOW INPUT TO CLEAR RESETS Q LOW AND Q HIGH REGARDLESS OF D-C LEVELS AT A OR B INPUT.

TIMING DIAGRAM



GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL MONOLITHIC MULTIVIBRATOR WITH A NEGATIVE-TRANSITION-TRIGGERED INPUT AND A POSITIVE-TRANSITION-TRIGGERED INPUT EITHER OF WHICH CAN BE USED AS AN INHIBIT INPUT.

PULSE TRIGGERING OCCURS AT A PARTICULAR VOLTAGE LEVEL AND IS NOT DIRECTLY RELATED TO THE TRANSITION TIME OF THE INPUT PULSE. SCHMITT-TRIGGER INPUT CIRCUITRY (TTL HYSTERESIS) FOR B INPUT ALLOWS JITTER-FREE TRIGGERING FROM INPUTS WITH TRANSITION RAYES AS SLOW AS 1 VOLT/SECOND.

ONCE FIRED, THE OUTPUTS ARE INDEPENDENT OF FURTHER TRANSITIONS OF THE A AND B INPUTS AND ARE A FUNCTION OF THE TIMING COMPONENTS, OR THE OUTPUT PULSES CAN BE TERMINATED BY THE OVERIDING CLEAR.

INPUT PULSES MAY BE OF ANY DURATION RELATIVE TO THE OUTPUT PULSE. OUTPUT PULSE LENGTH MAY BE VARIED FROM 35 NANOSECONDS TO 28 SECONDS BY CHOOSING THE APPROPRIATE TIMING COMPONENTS. WITH R_X = 2K OHMS AND C_X = 0 AN OUTPUT PULSE OF 30 NANOSECONDS IS TYPICALLY ACHIEVED. OUTPUT PULSE RISE AND FALL TIMES ARE TTL COMPATIBLE AND INDEPENDENT OF PULSE LENGTH
THE NOMINAL OUTPUT PULSE WIDTH IS DEFINED BY THE FOLLOWING EQUATION

$$T = C_X \times R_X \times \log_E 2$$

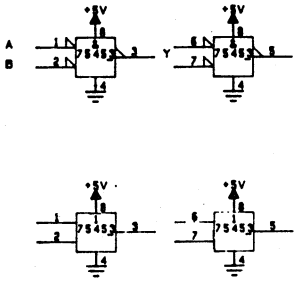
WHERE C_X = VALUE OF TIMING CAPACITOR

R_X = VALUE OF TIMING RESISTOR

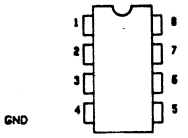
T = VALUE OF OUTPUT PULSE WIDTH

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 74221

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 76	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC Y=A•B

A	B	Y	
0	0	0	ON STATE
0	1	1	OFF STATE
1	0	1	OFF STATE
1	1	1	OFF STATE

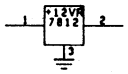
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL PERIPHERAL POSITIVE OR DRIVER (ASSUMING POSITIVE LOGIC) WITH THE OUTPUT OF THE LOGIC GATES INTERNALLY CONNECTED TO THE BASES OF THE N-P-N OUTPUT TRANSISTORS. THE CIRCUIT OUTPUT ARE OPEN COLLECTOR OUTPUTS.

TIMING DIAGRAM

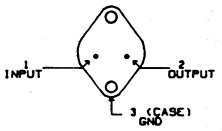
ELEMENT IDENTIFICATION #927
VENDOR IDENTIFICATION # 75453

SYMBOL/APPLICATION/PINS

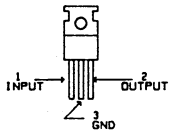


MECHANICAL CONFIGURATION (BOTTOM VIEW)

TO3 TYPE



TO220 TYPE



CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE (T_J=+25°C)	V_O	11.5	12	12.5	VDC
INPUT REGULATION (T_J=+25°C, I_O=100MA) 14.5VDC ≥ V_{IN} ≥ 30VDC 16VDC ≥ V_{IN} ≥ 22VDC (T_J=+25°C, I_O=500MA) 14.5VDC ≥ V_{IN} ≥ 30VDC 16VDC ≥ V_{IN} ≥ 22VDC	REG_{IN}		 13 6.0 55 24	 120 60 240 120	MV
LOAD REGULATION T_J=+25°C 5.0MA ≤ I_O ≤ 1.5A 250MA ≤ I_O ≤ 750MA	REG_{LOAD}		 46 17	 240 120	MV
OUTPUT VOLTAGE 14.5VDC ≥ V_{IN} ≥ 27VDC 5.0MA ≤ I_O ≤ 1.0A, P≤15W		11.4		12.6	VDC
QUIESCENT CURRENT (T_J=+25°C)	I_B		4.4	8.0	MA
QUIESCENT CURRENT CHG 14.5VDC ≥ V_{IN} ≥ 30VDC 5.0MA ≤ I_O ≤ 1.5MA	$\triangle I_B$			 1.0 0.5	MA
OUTPUT NOISE VOLTAGE (T_A=+25°C) (10HZ ≤ F ≤ 100HZ)	V_N		 75		UV
LONG-TERM STABILITY	$\Delta V_O / \Delta T$			48	MV 1.0K HRS
RIPPLE REJECTION I_O=20MA, F=120HZ	RR		61		DB
INPUT-OUTPUT VOLTAGE DIFFERENTIAL I_O=1.0A, T_J=+25°C	$V_{IN}-V_O$		2.0		VDC
AVG. TEM. COEF. OF OUTPUT VOLTAGE I_O=5.0MA, 0 C ≤ T_A ≤+125°C	TCV_O		-1.0		MV/°C

GENERAL OPERATIONAL DESCRIPTION

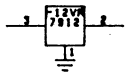
THIS DEVICE IS A THREE-TERMINAL POSITIVE VOLTAGE REGULATORS FOR A WIDE VARIETY OF APPLICATIONS INCLUDING LOCAL, ON-CARD REGULATION. AVAILABLE IN SEVEN FIXED OUTPUT VOLTAGE OPTIONS FROM 5.0 TO 24 VOLTS, THESE REGULATORS EMPLOY INTERNAL CURRENT LIMITING, THERMAL SHUTDOWN, AND SAFE AREA COMPENSATION-MAKING THEM ESSENTIALLY BLOW-OUT PROOF. WITH ADEQUATE HEATSINKING THEY CAN DELIVER OUTPUT CURRENTS IN EXCESS OF 1.0 AMPERE.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 7812

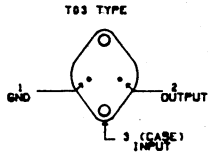
REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 78A	

KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)



REV	A	
DWG NO	95387500	
SHEET	77	
CODE IDENT	C	

KEY TO LOGIC SYMBOLS

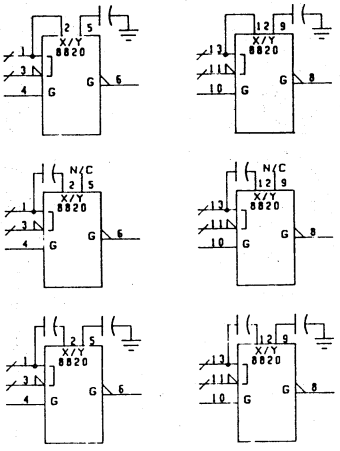
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE (T_J=+25°C)	V_O	-11.5	-12	-12.5	VDC
INPUT REGULATION (T_J=+25°C, I_O=100MA) -14.5VDC ≥ V_{IN} ≥-30VDC -16VDC ≥ V_{IN} ≥-22VDC (T_J=+25°C, I_O=500MA) -14.5VDC ≥ V_{IN} ≥-30VDC -16VDC ≥ V_{IN} ≥-22VDC	REG_{IN}		 13 6.0 55 24	 120 60 240 120	MV
LOAD REGULATION T_J=+25°C 5.0MA ≤ I_O ≤ 1.5A 250MA ≤ I_O ≤ 750MA	REG_{LOAD}		 46 17	 240 120	MV
OUTPUT VOLTAGE -14.5VDC ≥ V_{IN} ≥-27VDC 5.0MA ≤ I_O ≤ 1.0A, P≤15W		-11.4		-12.6	VDC
QUIESCENT CURRENT (T_J=+25°C)	T_B		4.4	8.0	MA
QUIESCENT CURRENT CHG 14.5VDC ≥ V_{IN} ≥ 30VDC 5.0MA ≤ I_O ≤ 1.5MA	$\triangle I_B$			 1.0 0.5	MA
OUTPUT NOISE VOLTAGE (T_A=+25°C) (10HZ ≤ F ≤ 10KHZ)	V_N		 75		UV
LONG-TERM STABILITY	$\triangle V_O / \triangle T$			48	MV/1.0K HRS
RIPPLE REJECTION I_O=28MA, F=120HZ	RR		61		DB
INPUT-OUTPUT VOLTAGE DIFFERENTIAL I_O=1.0A, T_J=+25°C	$V_{IN}-V_O$		2.8		VDC
AVG. TEM. COEF. OF OUTPUT VOLTAGE I_O=5.0MA, 0 C ≤ T_A ≤+125°C	TCV_O		-1.8		MV/°C

GENERAL OPERATIONAL DESCRIPTION

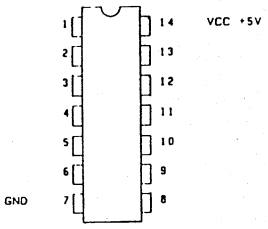
THIS DEVICE IS A THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS FOR A WIDE VARIETY OF APPLICATIONS INCLUDING LOCAL, ON-CARD REGULATION, AVAILABLE IN NINE FIXED OUTPUT VOLTAGE OPTIONS FROM -2.0 TO -24.0 VOLTS, THESE REGULATORS EMPLOY INTERNAL CURRENT LIMITING, THERMAL SHUTDOWN, AND SAFE AREA COMPENSATION-MAKING THEM ESSENTIALLY BLOW-OUT PROOF, WITH ADEQUATE HEATSINKING THEY CAN DELIVER OUTPUT CURRENTS IN EXCESS OF 1.0 AMPERE.

ELEMENT IDENTIFICATION #354G
VENDOR IDENTIFICATION #7912

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	F
DWG NO	95387500
CODE IDENT	C
SHEET 7 8	

KEY TO LOGIC SYMBOLS

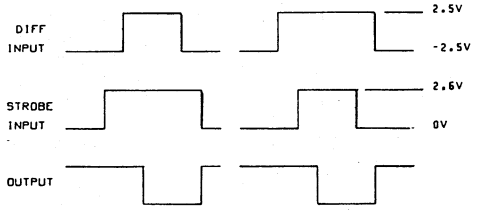
TRUTH TABLE

POS-LOGIC

INPUTS			OUTPUTS
4 10	1 13	3 11	6 8
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1
0	X	X	1

X = IRRELEVENT

TIMING DIAGRAM

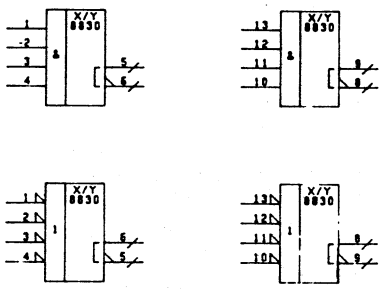


GENERAL OPERATIONAL DESCRIPTION

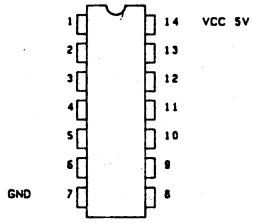
THESE DEVICES ARE DIGITAL LINE RECEIVERS WITH TWO COMPLETELY INDEPENDENT UNITS FABRICATED ON A SINGLE SILICON CHIP. THEY HAVE A DIFFERENTIAL INPUT DESIGNED TO REJECT LARGE COMMON MODE SIGNALS WHILE RESPONDING TO SMALL DIFFERENTIAL SIGNALS. THE OUTPUT IS DIRECTLY COMPATIBLE WITH RTL, DTL, OR TTL INTEGRATED CIRCUITS. THE RESPONSE TIME CAN BE CONTROLLED WITH AN EXTERNAL CAPACITOR TO ELIMINATE NOISE SPIKES, AND THE OUTPUT STATE IS DETERMINED FOR OPEN INPUTS. TERMINATION RESISTORS FOR THE TWISTED PAIR LINE ARE ALSO INCLUDED IN THE CIRCUIT.
THE TERMINATION INPUT (PINS 2 OR 12) MAY BE CONNECTED DIRECTLY TO THE INVERTING INPUTS (PINS 1 OR 13) OR MAY BE CONNECTED VIA A CAPACITOR FOR DC ISOLATION. A CAPACITOR MAY BE CONNECTED FROM THE RESPONSE TIME INPUT (PINS 5 OR 9) TO GROUND TO CONTROL THE RESPONSE TIME OF THE DEVICE.

ELEMENT IDENTIFICATION #910
VENDOR IDENTIFICATION #8820

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



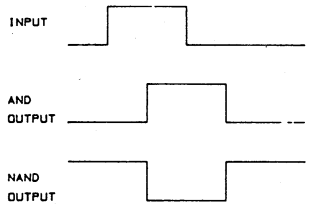
REV	A	
DWG NO	95387500	
CODE IDENT	C	SHEET 79

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUT PINS				OUTPUT PINS	
1 10	2 11	3 12	4 13	AND 5 9	NAND 6 8
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	0

TIMING DIAGRAM

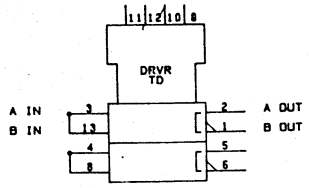


GENERAL OPERATIONAL DESCRIPTION

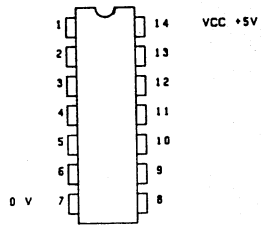
THIS IS A DUAL DIFFERENTIAL LINE DRIVER THAT ALSO PERFORMS THE DUAL FOUR-INPUT NAND OR DUAL FOUR-INPUT AND FUNCTION. THE DIFFERENTIAL OUTPUTS ARE BALANCED AND ARE DESIGNED TO DRIVE LONG LENGTHS OF COAXIAL CABLE, STRIP LINE, OR TWISTED PAIR TRANSMISSION LINES WITH CHARACTERISTIC IMPEDANCES OF 50 OHMS TO 500 OHMS.

ELEMENT IDENTIFICATION #909
VENDOR IDENTIFICATION #8830

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 80	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

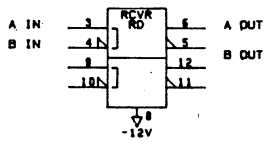
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL DIFFERENTIAL LINE DRIVER
THE RELATIONSHIP BETWEEN THE TWO INPUTS AND TWO OUTPUTS OF EACH ELEMENT SHALL BE SUCH THAT WITH BOTH INPUTS IN A HIGH STATE. OUTPUT A IS A HIGHER POTENTIAL THAN OUTPUT B. WITH EITHER OR BOTH INPUTS IN A LOW STATE. OUTPUT B IS AT A HIGHER POTENTIAL THAN OUTPUT A.
THIS DEVICE IS DESIGNED FOR USE IN CONJUNCTION WITH THE FC5 DEVICE.

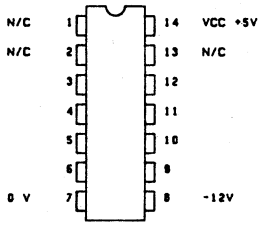
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # DRVR

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	C 95387500
SHEET	01
CODE IDENT	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

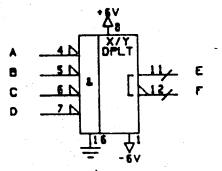
GENERAL OPERATIONAL DESCRIPTION

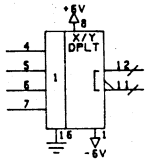
THIS DEVICE IS A DUAL DIFFERENTIAL LINE RECIEVER
EACH ELEMENT SHALL HAVE TWO INPUTS AND TWO OUTPUTS SO RELATED, THAT IF INPUT A IS POSITIVE, WITH RESPECT TO INPUT B, OUTPUT A IS HIGH AND OUTPUT B IS LOW.
WITH INPUT B POSITIVE WITH RESPECT TO INPUT A, OUTPUT A IS LOW AND OUTPUT B IS HIGH.
THIS DEVICE IS DESIGNED FOR USE IN CONJUNCTION WITH THE FC6 DEVICE.

TIMING DIAGRAM

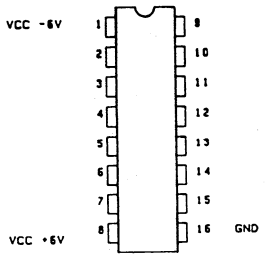
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # RCVR

SYMBOL/APPLICATION/PINS





MECHANICAL CONFIGURATION (TOP VIEW)



THIS DEVICE IS A FLAT PACK MOUNTED PACKAGE

REV	A
CODE IDENT	C
DWG NO	95387500
SHEET	02

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

A	B	C	D	E	F
1	X	X	X	L	H
X	1	X	X	L	H
X	X	1	X	L	H
X	X	X	1	L	H
0	0	0	0	H	L

1 = HIGH LOGIC LEVEL
0 = LOW LOGIC LEVEL
X = DON'T CARE
L = 0.5 VOLTS BELOW OTHER OUTPUT
H = 0.5 VOLTS ABOVE OTHER OUTPUT

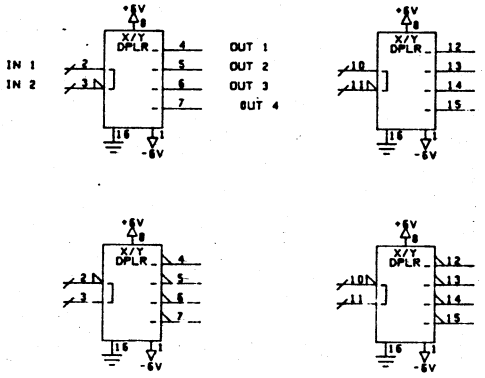
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

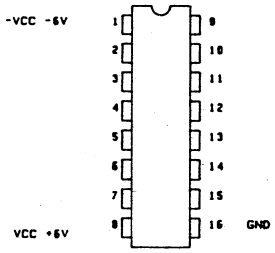
THIS DEVICE IS A DIFFERENTIAL PARTY LINE TRANSMITTER. AT THE OUTPUT PINS THERE IS A 0.5 VOLT DIFFERENTIAL BETWEEN THE TWO OUTPUTS.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #DPLT

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



THIS DEVICE IS A FLAT PACK MOUNTED PACKAGE

REV	A
DWG NO	95387500
CODE IDENT	C
SHEET 03	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

IN 1	IN 2	ALL OUTPUTS
L	H	0
H	L	1

L = 0.5 VOLTS BELOW OTHER INPUT
H = 0.5 VOLTS ABOVE OTHER INPUT
} DIFFERENTIAL
0 = LOW LOGIC LEVEL
1 = HIGH LOGIC LEVEL

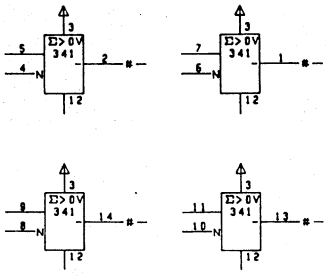
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DIFFERENTIAL PARTY LINE RECEIVER. A 0.5 VOLT DIFFERENTIAL SWING ON THE INPUTS WILL CAUSE A TTL LEVEL SWING ON ALL FOUR OUTPUTS. AS SHOWN IN THE TRUTH TABLE.

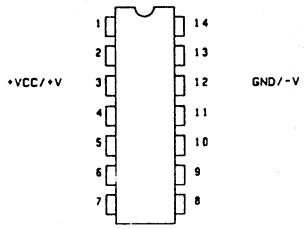
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # DPLR -

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGUCATION (TOP VIEW)



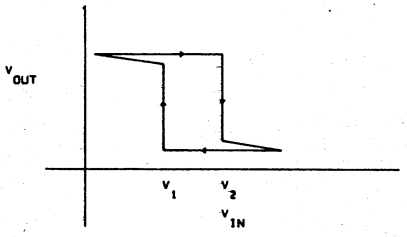
REV E
DWG NO 95387500
CODE IDENT C
SHEET 84
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

GENERAL OPERATIONAL DESCRIPTION

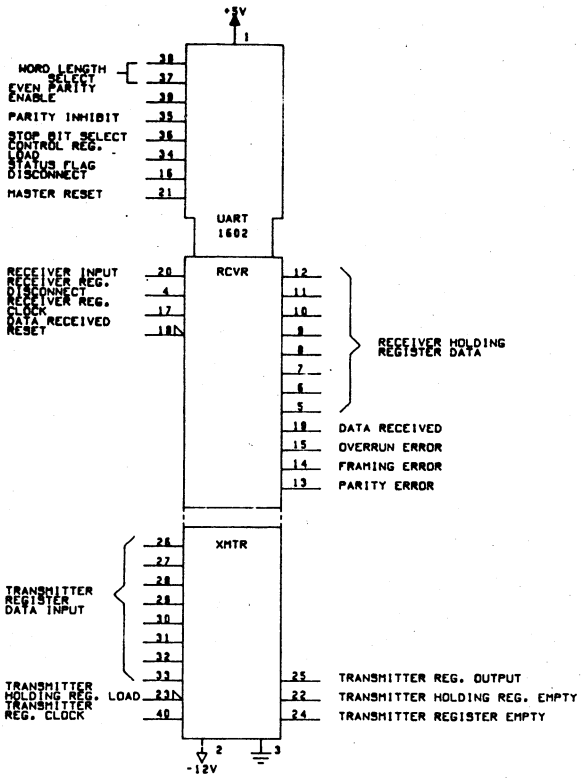
THIS CIRCUIT IS A VOLTAGE COMPARITOR. THE OUTPUT IS OPEN COLLECTOR AND TTL OR CMOS CONPATIBLE. THE INPUT VOLTAGE SENSING LEVELS ON BOTH POSITIVE AND NEGATIVE EXCURSIONS CAN BE SET BY EXTERNAL COMPONENTS. THE MAXIMUM INPUT OFFSET VOLTAGE IS 9.0 MVDC.

TIMING DIAGRAM

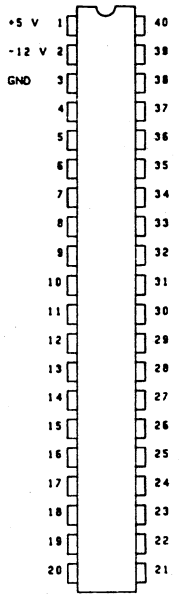


ELEMENT IDENTIFICATION #341
VENDOR IDENTIFICATION #LM339

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A

DWG NO 95387500

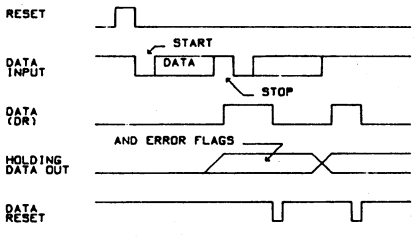
CODE IDENT C

SHEET 05

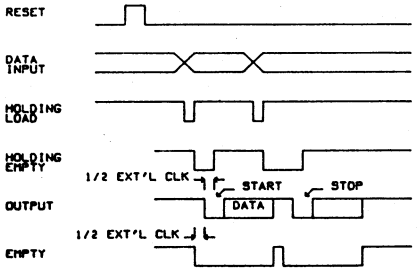
KEY TO LOGIC SYMBOLS

TRUTH TABLE
SEE DESCRIPTION

RECEIVER
TIMING DIAGRAM



TRANSMITTER
TIMING DIAGRAM

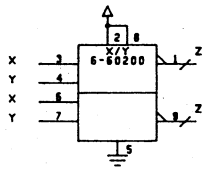


GENERAL OPERATIONAL DESCRIPTION

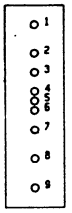
THIS DEVICE IS A UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER IN A SINGLE CHIP USED AS A PROGRAMMABLE MOS/LSI DEVICE FOR INTERFACING AN ASYNCHRONOUS SERIAL DATA CHANNEL OF A PERIPHERAL OR TERMINAL WITH PARALLEL DATA OF A COMPUTER OR TERMINAL. THE TRANSMITTER SECTION CONVERTS PARALLEL DATA INTO A SERIAL WORD WHICH CONTAINS THE DATA ALONG WITH START, PARITY, AND STOP BITS. THE RECEIVER SECTION CONVERTS A SERIAL WORD WITH START, DATA, PARITY, AND STOP BITS, INTO PARALLEL DATA, AND IT VERIFIES PROPER CODE TRANSMISSION BY CHECKING PARITY AND RECEIPT OF A VALID STOP BIT. BOTH THE RECEIVER AND THE TRANSMITTER ARE DOUBLE BUFFERED.
THE ARRAY IS COMPATIBLE WITH BIPOLAR LOGIC. THE ARRAY MAY BE PROGRAMMED AS FOLLOWS-- THE WORD LENGTH CAN BE EITHER 5, 6, 7, OR 8 BITS; PARITY GENERATION AND CHECKING MAY BE INHIBITED, THE PARITY MAY BE EVEN OR ODD; AND THE NUMBER OF STOP BITS MAY BE EITHER ONE OR TWO, WITH ONE AND ONE-HALF WHEN TRANSMITTING A 5 BIT CODE.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #TR1602A

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	05

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

INPUTS X	Y	OUTPUT Z
0	0	1
0	1	1
1	0	1
1	1	0

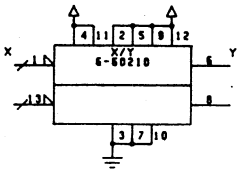
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL HYBRID TRANSMITTER DESIGNED FOR USE ON THE NCR MOS TRUNK. THE SUPPLY VOLTAGE (PINS 2 & 8) IS PROVIDED BY THE TRUNK. INPUTS TO THE TRANSMITTER ARE TTL COMPATIBLE. WHILE THE OUTPUT IS COMPATIBLE WITH MOS TRUNK LOGIC LEVELS.

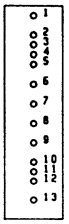
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #6-60200

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A	
DWG NO	95387500	
CODE IDENT	C	SHEET 87

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

INPUT X	OUTPUT Y
1	0
0	1

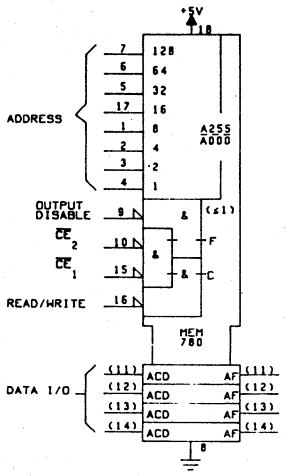
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL HYBRID RECEIVER DESIGNED FOR USE ON THE NCR MOS TRUNK. THE SUPPLY VOLTAGE IS SPLIT, WITH PINS 4 & 11 BEING SUPPLIED FROM THE TRUNK AND THE REMAINDER FROM THE PERIPHERAL. INPUTS TO THE RECEIVER ARE COMPATIBLE WITH THE MOS TRUNK, WHILE ITS OUTPUTS ARE TTL COMPATIBLE AND CAPABLE OF DRIVING 10 LOADS.

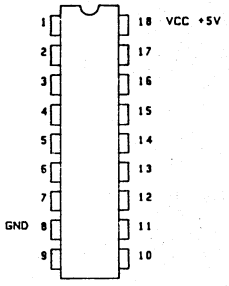
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #6-60210

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV A
DWG NO 9538750 0
CODE IDENT C
SHEET 8 8

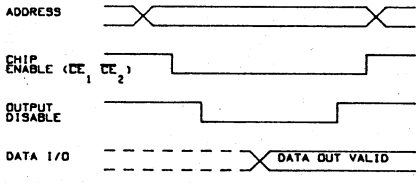
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

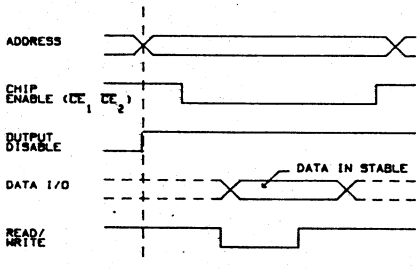
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A 256 WORD BY 4 BIT STATIC RANDOM ACCESS MEMORY. THE DATA IS READ OUT NONDESTRUCTIVELY AND HAS THE SAME LOGIC SENSE AS THE INPUT DATA. THE MEMORY IS FABRICATED WITH N-CHANNEL SILICON GATE TECHNOLOGY AND HAS TTL COMPATIBLE INPUTS AND OUTPUTS. THE OUTPUTS ARE THREE-STATE TO ALLOW OR-TIE CAPABILITY.

TIMING DIAGRAM
READ CYCLE

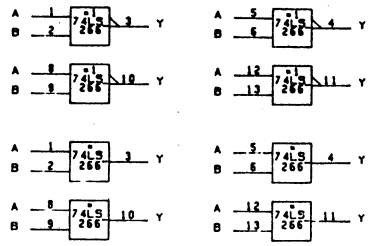


TIMING DIAGRAM
WRITE CYCLE

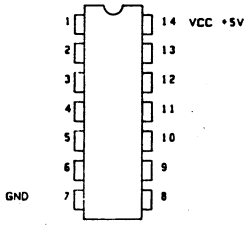


ELEMENT IDENTIFICATION 8708
VENDOR IDENTIFICATION 82111
8111
9111
TMS 4042

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	A
DWG NO	95387500
CODE IDENT	C
SHEET	88

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH LEVEL
L = LOW LEVEL

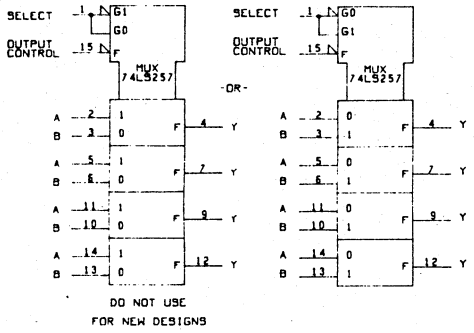
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS COMPRISED OF FOUR INDEPENDENT 2-INPUT EXCLUSIVE-NOR GATE WITH OPEN-COLLECTOR OUTPUTS. THE OPEN-COLLECTOR OUTPUTS PERMIT TYING OUTPUTS TOGETHER FOR MULTIPLE-BIT COMPARISONS

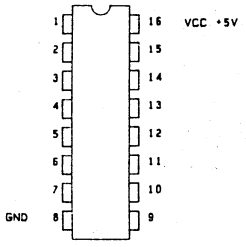
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #74LS266

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE
POS LOGIC

INPUTS				OUTPUT
OUTPUT CONTROL	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH LEVEL
L = LOW LEVEL
X = IRRELEVANT
Z = HIGH IMPEDANCE (OFF)

TIMING DIAGRAM

GENERAL OPERATION DESCRIPTION

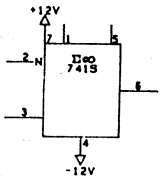
THIS DEVICE IS A QUAD 2-LINE TO 1-LINE MULTIPLEXER WITH THREE-STATE OUTPUTS THAT CAN INTERFACE DIRECTLY WITH AND DRIVE DATA LINES OF BUS-ORGANIZED SYSTEMS. WITH ALL BUT ONE OF THE COMMON OUTPUTS DISABLED (AT A HIGH-IMPEDANCE STATE) THE LOW IMPEDANCE OF THE SINGLE ENABLED OUTPUT WILL DRIVE THE BUS LINE TO A HIGH OR LOW LOGIC LEVEL. TO MINIMIZE THE POSSIBILITY THAT TWO OUTPUTS WILL ATTEMPT TO TAKE A COMMON BUS TO OPPOSITE LOGIC LEVEL, THE OUTPUT-ENABLE CIRCUITRY IS DESIGNED SUCH THAT THE OUTPUT DISABLE TIME ARE SHORTER THAN THE OUTPUT ENABLE TIMES.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #74LS257

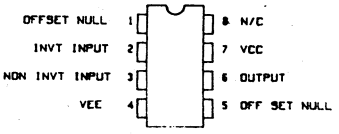
KEY TO LOGIC SYMBOLS

CODE IDENT C | DWG NO 95387500 | REV I | SHEET 90

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B
DWG NO	95387500
CODE IDENT	C
SHEET	81

KEY TO LOGIC SYMBOLS

TRUTH TABLE

TIMING DIAGRAM

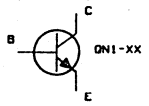
GENERAL OPERATIONAL DESCRIPTION

THE MC1741S/MC1741SC IS A HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER AND IS FUNCTIONALLY EQUIVALENT, PIN COMPATIBLE, AND POSSESSES THE SAME EASE OF USE AS THE POPULAR MC1741 CIRCUIT. YET OFFERS 20 TIMES HIGHER SLEW RATE AND POWER BANDWITH THIS DEVICE IS IDEALLY SUITED FOR D TO A CONVERTERS DUE TO ITS FAST SETTLING TIME AND HIGH SLEW RATE.

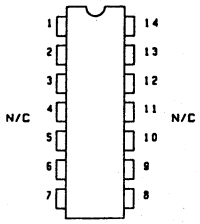
FEATURES OF THE MC1741S/MC1741SC ARE:
- HIGH SLEW RATE-10V/MS GUARANTEED MINIMUM (FOR UNITY GAIN)
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ELEMENT IDENTIFICATION # 741S
VENDOR IDENTIFICATION # MC1741S

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B
DWG NO	95387500
SHEET	02
CODE IDENT	C

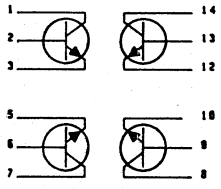
KEY TO LOGIC SYMBOLS

TRUTH TABLE

GENERAL OPERATIONAL DESCRIPTION

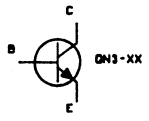
QUAD DUAL IN LINE NPN SILCON CORE DRIVER TRANSISTORS ARE DESIGNED FOR MEDIUM-CURRENT, HIGH SPEED SWITCHING AND DRIVER APPLICATIONS.

CIRCUIT DIAGRAM



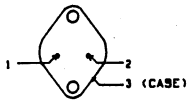
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # MPQ3725A
NETWORK IDENTIFICATION #ON1

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)

TO3 TYPE



1. BASE
2. EMITTER
3. (CASE) COLLECTOR

KEY TO LOGIC SYMBOLS	CODE IDENT	DWG NO	REV
	C	95387500	B
		SHEET 93	

TRUTH TABLE

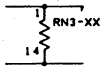
GENERAL OPERATIONAL DESRIPTION

DARLINGTON 20 AMPERE COMPLEMENTARY SILICON POWER TRANSISTOR IS DESIGNED FOR GENERAL PURPOSE AMPLIFIER AND LOW SPEED SWITCHING APPLICATIONS. THIS DEVICE HAS HIGH CURRENT GAIN WITH COLLECTOR EMITTER SUSTAINING VOLTAGE. IT IS A MONOLITHIC CONSTRUCTION WITH BUILT IN BASE-EMITTER SHUNT RESISTORS.

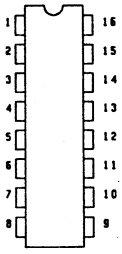
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 2N6282 THRU 2N6284 NPN
NETWORK IDENTIFICATION # QN3

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV B

DWG NO 95387500

CODE IDENT C

SHEET 94

KEY TO LOGIC SYMBOLS

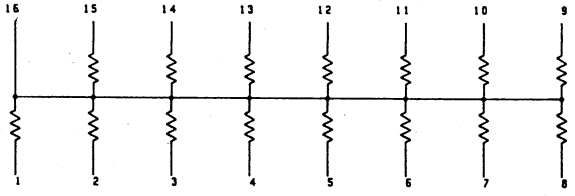
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

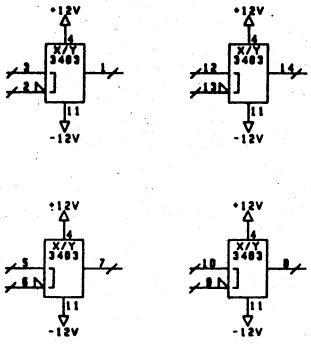
THIS DEVICE IS A DUAL-IN-LINE RESISTOR NETWORK ALL 15 RESISTORS IN THIS DEVICE ARE OF IDENTICAL VALUE WITH ONE COMMON CONNECTION. THIS VALUES SHALL BE DETERMINED AS PER THE DRAWING EMPLOYING THIS DEVICE.

CIRCUIT DIAGRAM

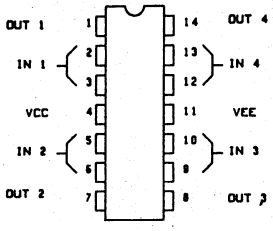


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 36C47
NETWORK IDENTIFICATION # RN3

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



CODE IDENT	C	DWG NO	95387500
			SHEET 85
		REV	B

KEY TO LOGIC SYMBOLS

TRUTH TABLE

TIMING DIAGRAM

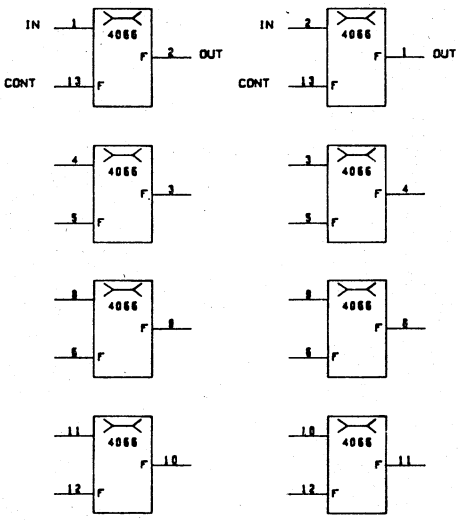
GENERAL OPERATIONAL DESCRIPTION

THE MC3503 IS A QUAD OPERATIONAL AMPLIFIER WITH TRUE DIFFERENTIAL INPUTS AND THIS QUAD AMPLIFIER CAN OPERATE AT SUPPLY VOLTAGES AS LOW AS 3.0 VOLTS OR AS HIGH AS 36 VOLTS WITH QUIESCENT CURRENTS AND THE COMMON MODE INPUT RANGE INCLUDES THE NEGATIVE SUPPLY, THEREBY ELIMINATING THE NECESSITY FOR EXTERNAL BIASING COMPONENTS IN MANY APPLICATIONS. THE OUTPUT VOLTAGE RANGE ALSO INCLUDES THE NEGATIVE POWER SUPPLY VOLTAGE. THE IMPORTANT CHARACTERISTICS OF THE DEVICE ARE:

SHORT CIRCUIT PROTECTED OUTPUTS, CLASS AB OUTPUT STAGE FOR MINIMAL CROSSOVER DISTORTION, TRUE DIFFERENTIAL INPUT STAGE, SINGLE SUPPLY OPERATION: 3.0 TO 36 VOLTS, SPLIT SUPPLY OPERATION: ±1.5 TO ±18 VOLTS, LOW INPUT BIAS CURRENTS: 500 NA MAX, FOUR AMPLIFIERS PER PACKAGE INTERNALLY COMPENSATED, SIMILAR PERFORMANCE TO POPULAR MC1741.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # MC3503L/MC3403PL

SYMBOL/APPLICATION/PINS



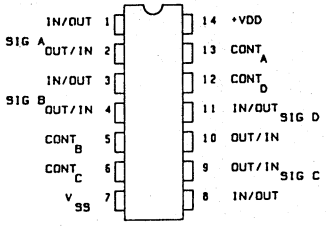
TRUTH TABLE

N/A

TIMING DIAGRAM

N/A

MECHANICAL CONFIGURATION (TOP VIEW)



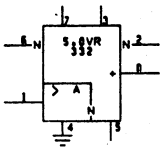
GENERAL OPERATIONAL DESCRIPTION

RCA-CD4066A IS A QUAD BILATERAL SWITCH INTENDED FOR THE TRANSMISSION OR MULTIPLEXING OF ANALOG OR DIGITAL SIGNALS. IT IS PIN FOR PIN COMPATIBLE WITH RCA-CD4016A, BUT INHIBITS A MUCH LOWER 'ON' RESISTANCE. IN ADDITION, THE 'ON' RESISTANCE IS RELATIVELY FIXED OVER THE FULL INPUT-SIGNAL RANGE. THE CD4066A CONSISTS OF FOUR INDEPENDENT BILATERAL SWITCHES. A SINGLE CONTROL SIGNAL IS REQUIRED PER SWITCH. BOTH THE 'P' AND THE 'N' DEVICE IN A GIVEN SWITCH ARE BIASED 'ON' OR 'OFF' BY THE CONTROL SIGNAL. THE WELL OF THE 'N' CHANNEL DEVISE ON EACH SWITCH IS EITHER TIED TO THE INPUT WHEN THE SWITCH IS ON OR VSS WHEN THE SWITCH IS 'OFF'. THIS CONFIGURATION ELIMINATES THE VARIATION OF THE SWITCH TRANSISTOR THRESHOLD VOLTAGE WITH INPUT SIGNAL, AND THUS KEEPS THE 'ON' RESISTANCE LOW OVER THE FULL OPERATING - SIGNAL RANGE. THE COS/MOS SWITCH PERMITS PEAK INPUT-SIGNAL VOLTAGE SWINGS EQUAL TO FULL SUPPLY VOLTAGE. A CONSIDERABLE ADVANTAGE OVER SINGLE-CHANNEL SWITCHES SOME SPECIAL FEATURES OF THE CD4066A ARE: WIDE RANGE OF DIGITAL ANALOG SIGNAL LEVELS: DIGITAL OR ANALOG SIGNAL TO 15V PEAK ANALOG SIGNAL ±7.5V PEAK, LOW 'ON' RESISTANCE: 100 OHM TYP. OVER 15VP-P SIGNAL INPUT RANGE, FOR VDD-VSS = 15V, MATCHED SWITCH CHARACTERISTICS: 5 OHM TYP. DIFFERENCE BETWEEN R_{ON} VALUES AT A FIXED BIAS POINT OVER 15VP-P SIGNAL INPUT RANGE, VDD -VSS = 15V, HIGH ON/OFF OUTPUT VOLTAGE RATIO:65 DB TYP. @ F_{IS}=10KHZ, R_L=10KOHM, HIGH DEGREE OF LINEARITY, EXTREMELY LOW 'OFF' SWITCH LEAKAGE RESULTING IN VERY LOW OFFSET CURRENT AND HIGH EFFECTIVE 'OFF' RESISTANCE, EXTREMELY HIGH CONTROL INPUT INPEDANCE, LOW CROSS TALK BETWEEN SWITCHES, MATCHED CONTROL-INPUT TO SIGNAL-OUTPUT CAPACITANCE, TRANSMITS FREQUENCIES UP TO 18MHZ.

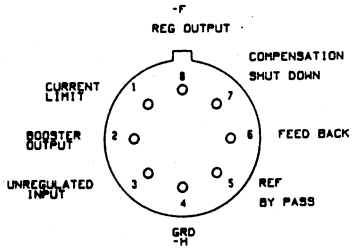
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # CD4066A

REV B
DWG NO 95387500
CODE IDENT C
SHEET 86
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)



NOTE: PIN 4 CONNECTED TO BOTTOM OF PACKAGE

REV B

DWG NO 95387500

CODE IDENT C

SHEET 07

KEY TO LOGIC SYMBOLS

TRUTH TABLE

N/A

TIMING DIAGRAM

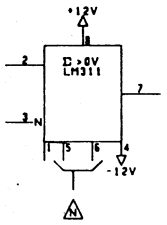
N/A

GENERAL OPERATIONAL DESCRIPTION

THE LM105, LM205, LM305 ARE POSITIVE VOLTAGE REGULATORS WITH AN EXTRA GAIN STAGE FOR IMPROVED REGULATION. THIS CIRCUITRY REMOVES ANY MINIMUM LOAD CURRENT REQUIREMENT AND AT THE SAME TIME REDUCES STAND BY CURRENT DRAIN, PERMITTING HIGHER VOLTAGE OPERATION. THEY ARE DIRECT, PLUG IN REPLACEMENTS FOR THE LM100 IN BOTH LINEAR AND SWITCHING REGULATOR CIRCUITS WITH OUTPUT VOLTAGES GREATER THAN 4.5V. IMPORTANT CHARACTERISTICS OF THE CIRCUITS ARE: OUTPUT VOLTAGE ADJUSTABLE FROM 4.5V TO 43V, OUTPUT CURRENT IN EXCESS OF 10A POSSIBLE BY ADDING EXTERNAL TRANSISTORS, LOAD REGULATION BETTER THAN 0.1%, FULL LOAD WITH CURRENT LIMITING, DC LINE REGULATION GUARANTEED AT 0.03%/V RIPPLE REJECTION OF 0.01%/V, LIKE THE LM100, THEY ALSO FEATURE FAST RESPONSE TO BOTH LOAD AND LINE TRANSIENTS, FREEDOM FROM OSCILLATIONS WITH VARYING RESISTIVE AND REACTIVE LOADS AND THE ABILITY TO START RELIABLY ON ANY LOAD WITH RATING.

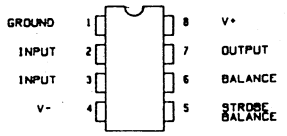
ELEMENT IDENTIFICATION # 332
VENDOR IDENTIFICATION #LM105H, LM205H
LM305H

SYMBOL/APPLICATION/PINS



-NULL INPUT

MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE

N/A

TIMING DIAGRAM

N/A

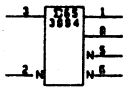
GENERAL OPERATIONAL DESCRIPTION

THE LM311 IS A VOLTAGE COMPARATOR THAT HAS INPUT CURRENTS MORE THAN A HUNDRED TIMES LOWER THAN DEVICES LIKE THE LM306 OR LM710C. IT IS ALSO DESIGNED TO OPERATE OVER A WIDER RANGE OF SUPPLY VOLTAGES: FROM STANDARD ±15V OP AMP SUPPLIES DOWN TO THE SINGLE 5V SUPPLY USED FOR IC LOGIC. ITS OUTPUT IS COMPATIBLE WITH RTL, DTL, AND TTL AS WELL AS MOS CIRCUITS. FURTHER, IT CAN DRIVE LAMPS OR RELAYS, SWITCHING VOLTAGE UP TO 40V AT CURRENTS AS HIGH AS 50MA. THE DEVICE CHARACTERISTICS ARE: OPERATES FROM SINGLE 5V SUPPLY, MAXIMUM INPUT CURRENT: 250NA: MAXIMUM OFFSET CURRENT: 50NA: DIFFERENTIAL INPUT VOLTAGE RANGE: ±30V: POWER CONSUMPTION: 135MW AT ±15V. BOTH THE INPUT AND THE OUTPUT OF THE LM311 CAN BE ISOLATED FROM SYSTEM GROUND, AND THE OUTPUT CAN DRIVE LOADS REFERRED TO GROUND, THE POSITIVE SUPPLY OR THE NEGATIVE SUPPLY. OFFSET BALANCING AND STROBE CAPABILITY ARE PROVIDED AND OUTPUTS CAN BE WIRE OR'ED. ALTHOUGH SLOWER THAN THE LM306 AND LM710C (200NS RESPONSE VS 40 NS) THE DEVICE IS ALSO LESS PRONE TO SPURIOUS OSCILLATIONS. THE LM311 HAS THE SAME PIN CONFIGURATION AS THE LM306 AND LM710C.

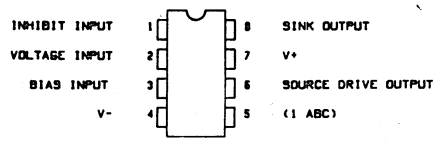
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # LM311

REV B
DWG NO 95387500
CODE IDENT C
SHEET 98
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B
DWG NO	95387500
CODE IDENT	C
SHEET	88

KEY TO LOGIC SYMBOLS

TRUTH TABLE

OUTPUT MODE	OUTPUT TERM.	INPUTS	
		INV.	NON-INV.
SOURCE	6	2	3
SINK	8	3	2

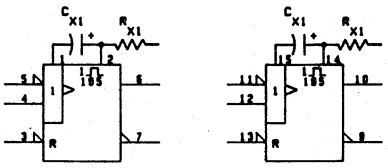
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

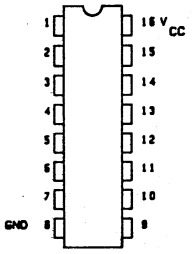
THE CA3094 IS A DIFFERENTIAL-INPUT POWER-CONTROL SWITCH/AMPLIFIER WITH AUXILIARY CIRCUIT FEATURES FOR EASE OF PROGRAMMABILITY. FOR EXAMPLE, AN ERROR OR UNBALANCE SIGNAL CAN BE AMPLIFIED BY THE CA3094 TO PROVIDE AN ON-OFF SIGNAL OR PROPORTIONAL-CONTROL OUTPUT SIGNAL UP TO 100MA. THIS SIGNAL IS SUFFICIENT TO DIRECTLY DRIVE HIGH-CURRENT THYRISTORS, RELAYS, DC LOADS, OR POWER TRANSISTORS. THE CA3094 HAS THE GENERAL CHARACTERISTICS OF THE RCA CA3080 OPERATIONAL AMPLIFIER DIRECTLY COUPLED TO AN INTEGERAL DARLINGTON POWER TRANSISTOR CAPABLE OF SINKING OR DRIVING CURRENTS UP TO 100MA. THE GAIN OF THE DIFFERENTIAL INPUT STAGE IS PROPORTIONAL TO THE AMPLIFIER BIAS CURRENT (1 ABC) PERMITTING PROGRAMMABLE VARIATION OF THE INTEGRATED CIRCUIT SENSITIVITY WITH EITHER DIGITAL AND/OR ANALOG PROGRAMMING SIGNALS. FOR EXAMPLE, AT AN I ABC OF 100 UA A ONE MILLIVOLT CHANGE AT THE INPUT WILL CHANGE THE OUTPUT FROM 0 TO 100MA (TYPICAL). THE CA3094 IS INTENDED FOR OPERATION UP TO 24 VOLTS IS A PRIMARY DESIGN REQUIREMENT. THE CA3094A AND CA3094B ARE LIKE THE CA3094 BUT ARE INTENDED FOR OPERATION UP TO 36 AND 44 VOLTS, RESPECTIVELY (SINGLE OR DUAL SUPPLY). THE CHARACTERISTICS ARE DESIGNED FOR SINGLE OR DUAL POWER SUPPLY; PROGRAMMABLE; STROBING, GATING, SQUELCHING, AGC CAPABILITIES; CAN DELIVER 3 WATTS (AVG) OR 10 W (PEAK) TO EXTERNAL LOAD (IN SWITCHING MODE); HIGH POWER, SINGLE-ENDED CLASS A AMPLIFIER WILL DELIVER POWER OUTPUT OF 0.6 WATT (1.6 W DEVICE DISSAPATION); TOTAL HARMONIC DISTORTION (THD) @ 0.6 W IN CLASS A OPERATION- 1.4% TYP.; HIGH CURRENT-HANDLING CAPABILITY- 100MA (AVG) 300MA (PEAK); SENSITIVITY CONTROLLED BY VARYING BIAS CURRENT; OUTPUT; SINK OR DRIVE CAPABILITY.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # CA3094E

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B
DWG NO	95387500
CODE IDENT	C
SHEET	100

KEY TO LOGIC SYMBOLS

TRUTH TABLE

TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
3,4,5,11 12,13,	1 UL	1 UL

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6,7,8,10	16 UL	8 UL

1 UNIT LOAD (UL) = 50UA/16MA LOW

PIN NO'S			OPERATION
5(11)	4(12)	3(13)	
H - L	L	H	TRIGGER
H	L - H	H	TRIGGER
X	X	L	RESET

TIMING DIAGRAM

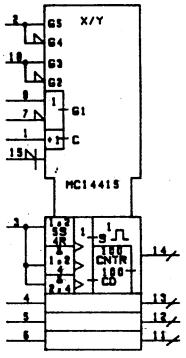
N/A

GENERAL OPERATIONAL DESCRIPTION

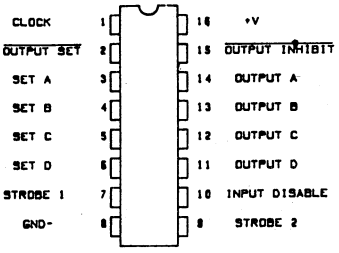
THE TTL/MONOSTABLE DM 8602/DM 8602 DUAL RETRIGGERABLE, RESETTABLE MONOSTABLE MULTIVIBRATOR PROVIDES AN OUTPUT PULSE WHOSE DURATION AND ACCURACY IS A FUNCTION OF EXTERNAL TIMING COMPONENTS. THIS DEVICE HAS EXCELLENT IMMUNITY TO NOISE ON THE V_{CC} AND GROUND LINES. IT USES TTL INPUTS AND OUTPUTS FOR HIGH SPEED AND HIGH FANOUT CAPABILITY AND IS COMPATIBLE WITH ALL MEMBERS OF THE TTL FAMILY.

ELEMENT IDENTIFICATION # 185
VENDOR IDENTIFICATION # DM 8602

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



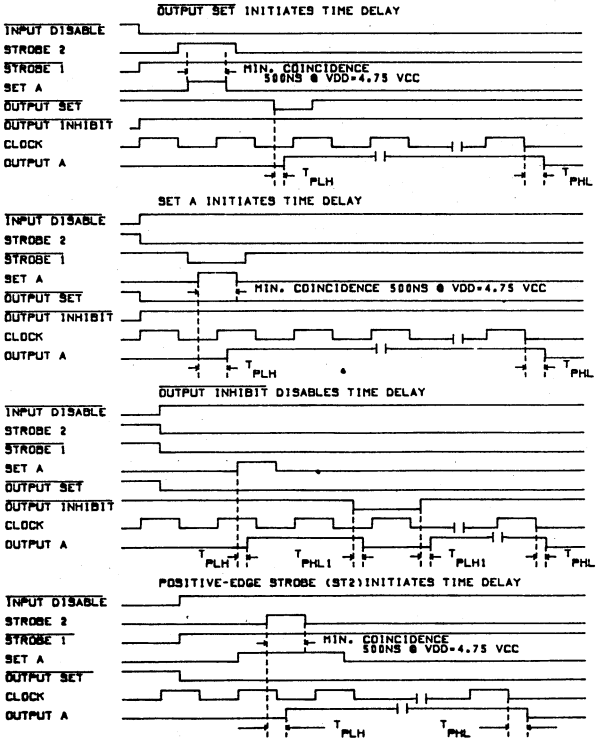
CODE IDENT	DWG NO	REV
C	95387500	G

SHEET 101

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

TIMING DIAGRAG



GENERAL OPERATIONAL DESCRIPTION

THE MC14415 QUAD TIMER/DRIVER IS CONSTRUCTED WITH COMPLEMENTART MOS ENHANCEMENT MODE DEVICES. THE OUTPUT PULSE WIDTH OF EACH DIGITAL TIMER IS A FUNCTION OF THE INPUT CLOCK FREQUENCY. ONCE THE PROPER INPUT SEQUENCE IS DETECTED THE OUTPUT BUFFER IS SET (TURNED ON), AND 100 CLOCK PULSES ARE COUNTED, THE OUTPUT BUFFER IS RESET (TURNED OFF).

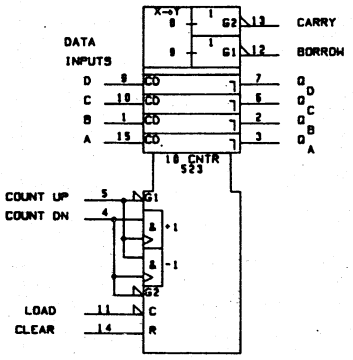
THE MC14415 WAS DESIGNED SPECIFICALLY FOR APPLICATION IN HIGH SPEED LINE PRINTERS TO PROVIDE THE CRITICAL TIMING OF THE HAMMER DRIVERS, BUT MAY BE USED IN MANY APPLICATIONS REQUIRING PRECISION WIDTHS.

FEATURES IN THE MC14415:

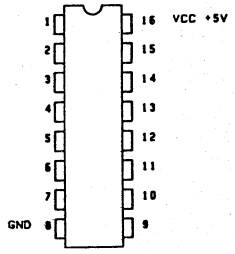
- FOUR PRECISION DIGITAL TIME DELAYS
- SCHMITT TRIGGER CLOCK CONDITIONING
- NPN BIPOLAR OUTPUT DRIVERS
- TIMING DISABLE CAPABILITY USING INHIBIT OUTPUT
- POSITIVE OR NEGATIVE EDGE STROBING ON THE INPUTS
- SYNCHRONOUS POLYNOMINAL COUNTERS USED FOR DELAY COUNTING
- POWER SUPPLY OPERATING RANGE
  - +3.0 VDC TO 18 VDC (MC14415EFL)
  - +3.0 VDC TO 16 VDC (MC14415FL/FP)
  - +3.0 VDC TO 6.0 VDC (MC14415EVL/VL/VP)

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # MC14415VP

SYMBOL/APPLICATION/PINS



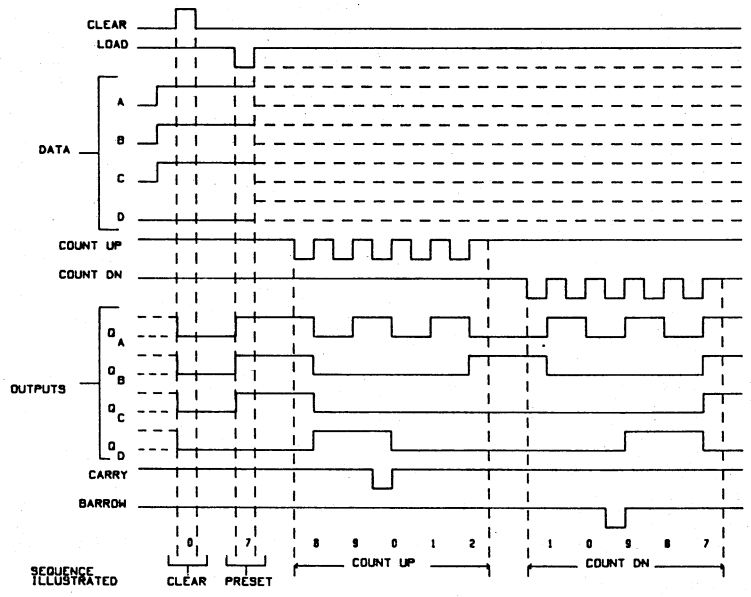
MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE
POS-LOGIC SEE DESCRIPTION

TIMING DIAGRAM
DECADE COUNTER (TYPICAL CLEAR, LOAD, AND COUNT SEQUENCE)

1. CLEAR OUTPUTS TO ZERO
2. LOAD (PRESET) TO BCD SEVEN.
3. COUNT UP TO EIGHT, NINE, CARRY, ZERO, ONE AND TWO.
4. COUNT DOWN ONE, ZERO, BORROW, NINE, EIGHT AND SEVEN.



NOTES

A. CLEAR OVERIDES LOAD, DATA, AND COUNT INPUTS.
B. WHEN COUNTING UP COUNT DOWN INPUTS MUST BE HIGH.
WHEN COUNTING DOWN, COUNT UP INPUTS MUST BE HIGH.

GENERAL OPERATIONAL DESCRIPTION

THIS IS A SYNCHRONOUS (UP/DOWN) COUNTER HAVING A COMPLEXITY OF 55 EQUIVALENT GATES. THE SS4192 AND N74192 ARE BCD COUNTERS. SYNCHRONOUS OPERATION IS PROVIDED BY HAVING ALL FLIP-FLOPS CLOCKED SIMULTANEOUSLY SO THAT THE OUTPUTS CHANGE COINCIDENTLY WITH EACH OTHER WHEN SO INSTRUCTED BY STEERING LOGIC. THIS MODE OF OPERATION ELIMINATES THE OUTPUT COUNTING SPIKES WHICH ARE NORMALLY ASSOCIATED WITH ASYNCHRONOUS (RIPPLE-CLOCK) COUNTERS.

THE OUTPUTS OF THE MASTER-SLAVE FLIP-FLOPS ARE TRIGGERED BY A LOW-TO-HIGH-LEVEL TRANSISTION OF EITHER COUNT (CLOCK) INPUT. THE DIRECTION OF COUNTING IS DETERMINED BY WHICH COUNT INPUT IS PULSED WHILE THE OTHER COUNT INPUT IS HIGH.

THESE COUNTERS ARE FULLY PROGRAMMABLE; THAT IS, THE OUTPUTS MAYBE PRESENTED TO ANY STATE BY ENTERING THE DESIRED DATA AT THE DATA INPUTS WHILE THE LOAD INPUT IS LOW. THE OUTPUT WILL CHANGE TO AGREE WITH THE DATA INPUTS INDEPENDENTLY OF THE COUNT PULSES. THIS FEATURE ALLOWS THE COUNTER TO BE USED AS MODULO-N DEVIDERS BY SIMPLY MODIFYING THE COUNT LENGTH WITH THE PRESET INPUTS.

A CLEAR INPUT HAS BEEN PROVIDED WHICH FORCES ALL OUTPUTS TO THE LOW LEVEL WHEN A HIGH LEVEL IS APPLIED. THE CLEAR FUNCTION IS INDEPENDENT OF THE COUNT AND LOAD INPUTS. THE CLEAR, COUNT AND LOAD INPUTS ARE BUFFERED TO LOWER THE DRIVER REQUIREMENTS TO ONE NORMALIZED SERIES 54/74 LOAD. THIS IS IMPORTANT WHEN THE OUTPUT OF THE DRIVING CIRCUITRY IS SOMEWHAT LIMITED.

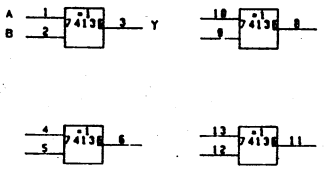
THESE COUNTERS WERE DESIGNED TO BE CASCADED WITHOUT THE NEED FOR EXTERNAL CIRCUITRY. BOTH BORROW AND CARRY OUTPUTS ARE AVAILABLE TO CASCADE BOTH UP-AND DOWN-COUNTING FUNCTION. THE BORROW OUTPUT PROVIDES A PULSE EQUAL IN WIDTH TO THE COUNT-DOWN INPUT WHEN THE COUNTERS UNDERFLOWS. SIMILARY, THE CARRY OUTPUT PRODUCES A PULSE EQUAL IN WIDTH TO THE COUNT UP INPUT WHEN AN OVERFLOW CONDITION EXISTS. THE COUNTERS CAN THEN BE EASILY CASCADED BY FEEDING THE BORROW AND CARRY OUTPUTS TO THE COUNT-DOWN AND COUNT-UP INPUTS RESPECTIVELY OF THE SUCCEEDING COUNTER.

ELEMENT IDENTIFICATION # 523
VENDOR IDENTIFICATION # 74192

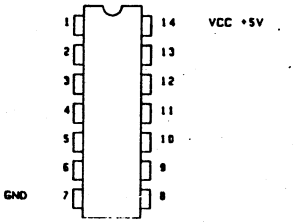
KEY TO LOGIC SYMBOLS

CODE IDENT C | DWG NO 95387500 | REV B | SHEET 102

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV: B

DWG NO 95387500

SHEET 103

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH LEVEL
L = LOW LEVEL

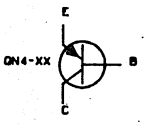
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

THIS QUADRUPLE 2 INPUT EXCLUSIVE-OR GATE, WITH OPEN COLLECTOR OUTPUT UTILIZES TTL CIRCUITRY TO PRFORM THE FUNCTION $Y=A\overline{B}+\overline{A}B$. WHEN THE INPUT STATES ARE COMPLEMENTARY, THE OUTPUT GOES TO A LOGICAL 1.

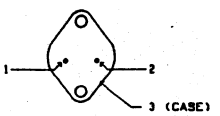
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # SN74136

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)

T03 TYPE



1. BASE
2. EMITTER
3. (CASE) COLLECTOR

REV	B
DWG NO	9538750
CODE IDENT	C
SHEET 104	

KEY TO LOGIC SYMBOLS

TRUTH TABLE

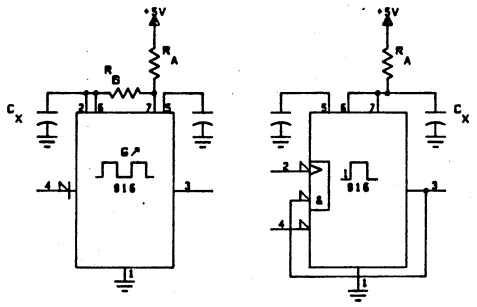
GENERAL OPERATIONAL DESCRIPTION

DARLINGTON 20 AMPHERE COMPLEMENTARY SILICON POWER TRANSISTOR IS DESIGNED FOR GENERAL PURPOSE AMPLIFIER AND LOW SPEED SWITCHING APPLICATIONS. THIS DEVICE HAS HIGH CURRENT GAIN WITH COLLECTOR EMITTER SUSTAINING VOLTAGE. IT IS A MONOLITHIC CONSTRUCTION WITH BUILT IN BASE-EMITTER SHUNT RESISTORS.

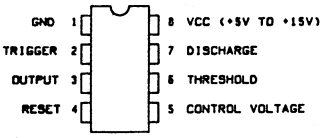
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 2N6285 THRU 2N6287 PNP
NETWORK IDENTIFICATION #QN4

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)

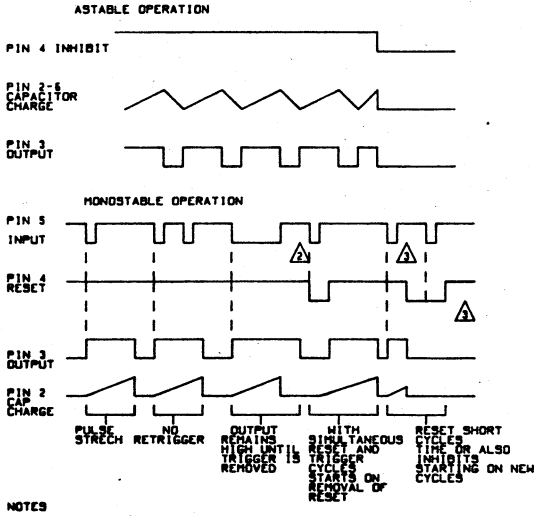


REV	B
DWG NO	95387500
SHEET	105
CODE IDENT	C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

TIMING DIAGRAM



NOTES

1. THIS DEVICE WILL NOT FUNCTION AS A PULSE SHRINKER.
2. THESE EDGES ARE AT THE SAME TIME
3. THERE WILL BE NO TRIGGERING EVEN AFTER REMOVAL OF THE RESET, BECAUSE THE INPUTS OCCURED DURING RESET.

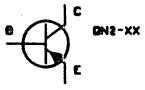
GENERAL OPERATIONAL DESCRIPTION

THIS NE/SE MONOLITHIC TIMING CIRCUIT IS A HIGHLY STABLE CONTROLLER CAPABLE OF PRODUCING ACCURATE TIME DELAY, OR OSCILLATION. ADDITIONAL TERMINALS ARE PROVIDED FOR TRIGGERING OR RESETTING IF DESIRED. IN THE TIME DELAY MODE OF OPERATION, THE TIME IS PRECISELY CONTROLLED BY ONE EXTERNAL RESISTOR AND CAPACITOR. $T_D = .693 (R_A + R_B) C_X$

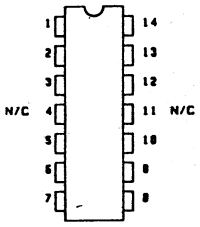
$C_X = \frac{T}{(.693)(R_A + R_B)}$ THE CIRCUIT MAY BE TRIGGERED AND RESET ON FALLING WAVE FORMS, AND THE OUTPUT STRUCTURE CAN SOURCE OR SINK UP TO 200MA OR DRIVE TTL CIRCUITS.

ELEMENT IDENTIFICATION # 816
VENDOR IDENTIFICATION #555

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B
DWG NO	95387500
SHEET	106
CODE IDENT	C

KEY TO LOGIC SYMBOLS

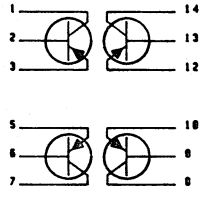
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

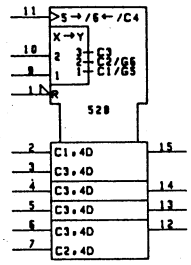
THE MHQ 3700 QUAD DUAL-IN-LINE PNP HERMETIC SILICON ANNULAR AMPLIFIER TRANSISTORS ARE DESIGNED FOR LOW LEVEL LOW NOISE AMPLIFIER APPLICATIONS. SOME CHARACTERISTICS ARE: LOW DC CURRENT GAIN SPECIFIED-10 UA DC TO 10 MA DC. LOW CAPACITANCE. LOW NOISE FIGURE-NF=2.5 DB (TYP @ I_C=100 UA DC. TRANSISTORS ARE SIMILAR TO 2N3700 AND 2N3700

CIRCUIT DIAGRAM

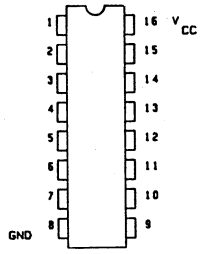


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # MHQ3700
NETWORK IDENTIFICATION # QN2

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THESE BIDIRECTIONAL SHIFT REGISTERS ARE DESIGNED TO INCORPORATE VIRTURALLY ALL OF THE FEATURES A SYSTEM DESIGNER MAY WANT IN A SHIFT REGISTER. THE CIRCUIT CONTAINS 46 EQUIVALENT GATES AND FEATURES PARALLED INPUTS, PARALLEL OUTPUTS, RIGHT SHIFT AND LEFT SHIFT SERIAL INPUTS, OPERATING-MODE-CONTROL INPUTS, AND A DIRECT OVERRIDING CLEAR LINE. THE REGISTER HAS FOUR DISTINCT MODES OF OPERATION, NAMELY:

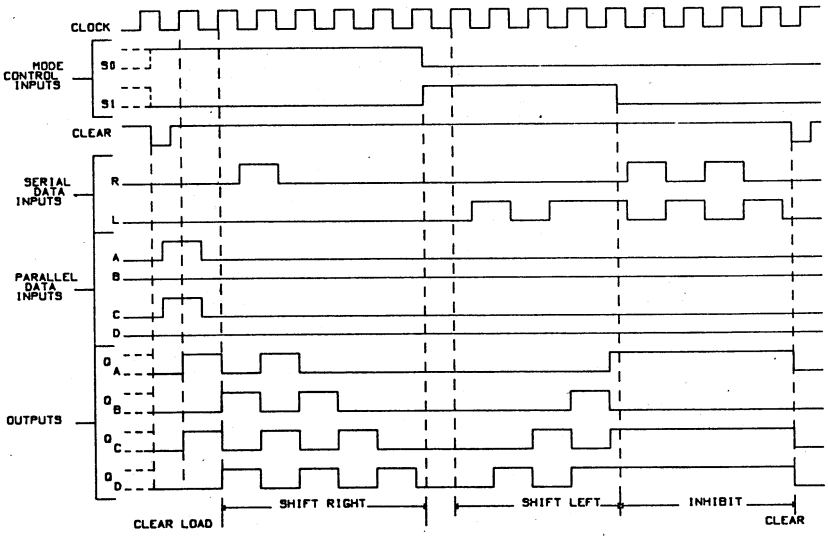
TRUTH TABLE

	MODE CONTROL	
	S1	S0
PARALLEL (BROADSIDE)LOAD	H	H
SHIFT RIGHT (IN DIRECTION Q_A TOWARD Q_D)	L	H
SHIFT LEFT (IN DIRECTION Q_D TOWARD Q_A)	H	L
INHIBIT CLOCK (DO NOTHING)	L	L

IN THE PARALLEL MODE, DATA IS LOADED INTO THE ASSOCIATED FLIP-FLOP AND APPEARS AT THE OUTPUTS AFTER THE POSITIVE TRANSISTION OF THE CLOCK INPUT. DURING LOADING, SERIAL DATA FLOW IS INHIBITED. SHIFT RIGHT IS ACCOMPLISHED SYNCHRONOUSLY WITH THE RISING EDGE OF THE CLOCK PULSE WHEN S0 IS HIGH AND S1 IS LOW. SERIAL DATA FOR THIS MODE IS ENTERED AT THE SHIFT RIGHT DATA INPUT. WHEN S0 IS LOW AND S1 IS HIGH, DATA SHIFT LEFT SYNCHRONOUSLY AND NEW DATA IS ENTERED AT THE SHIFT-LEFT SERIAL INPUT. CLOCKING OF THE FLIP-FLOPS IS INHIBITED WHEN BOTH MODE CONTROLS SHOULD BE CHANGED ONLY WHILE CLOCK INPUT IS HIGH

THESE FOUR BIT SHIFT REGISTERS ARE COMPATIBLE WITH MOST OTHER TTL AND DTL LOGIC FAMILIES. ALL INPUTS ARE BUFFERED TO LOWER THE DRIVE REQUIREMENTS TO ONE NORMILIZED SERIES 54/74 LOAD, AND INPUT CLAMPING DIODES MINIMIZE SWITCHING TRANSIENTS TO SIMPLIFY SYSTEM DESIGN. MAXIMUM INPUT CLOCK FREQUENCY IS TYPICALLY 36 MEGAHERTZ AND POWER DISSIAPATION IS TYPICALLY 195 MW

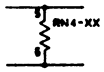
TIMING DIAGRAM



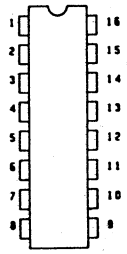
ELEMENT IDENTIFICATION # 528
VENDOR IDENTIFICATION # 74194

REV B
CODE IDENT C
DWG NO 9538750O
SHEET 107
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV B

DWG NO 95387500

SHEET 108

CODE IDENT C

KEY TO LOGIC SYMBOLS

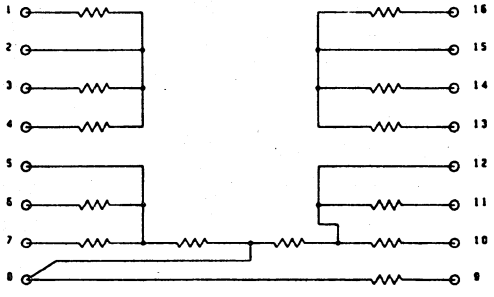
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

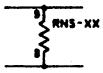
THIS DEVICE IS AN IN-LINE RESISTOR NETWORK. IT CONSISTS OF 13 RESISTORS OF VARIOUS VALUES. THESE VALUES SHALL BE DETERMINED AS PER THE DRAWING EMPLOYING THIS DEVICE.

CIRCUIT DIAGRAM

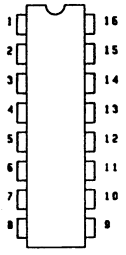


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # RS071675
NETWORK IDENTIFICATION # RN4

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



CODE IDENT	C	DWG NO 95387500	REV B
		SHEET 100	

KEY TO LOGIC SYMBOLS

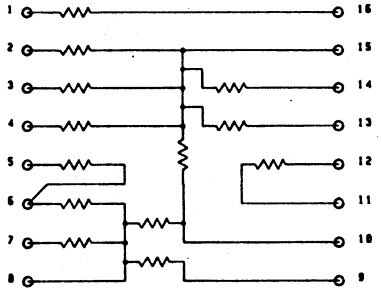
TIMING DIAGRAM

N/A

GENERAL OPERATIONAL DESCRIPTION

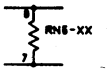
THIS DEVICE IS A SINGLE-IN-LINE RESISTOR NETWORK . IT CONSISTS OF 13 RESISTORS OF VARIOUS VALUES. THESE VALUES SHALL BE DETERMINED AS PER DRAWINGS EMPLOYING THIS DEVICE.

CIRCUIT DIAGRAM

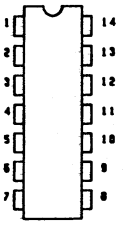


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # HA120875
NETWORK IDENTIFICATION # RNS

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B
DWG NO	95387500
CODE IDENT	C
SHEET 110	

KEY TO LOGIC SYMBOLS

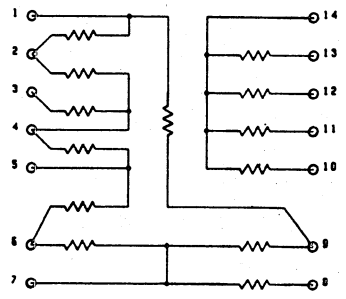
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

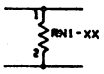
THIS DEVICE IS A SINGLE-IN-LINE RESISTOR NETWORK. IT CONSISTS OF 13 RESISTORS OF DIFFERENT VALUES. THESE VALUES SHALL BE DETERMINED AS PER DRAWINGS EMPLOYING THIS DEVICE.

CIRCUIT DIAGRAM

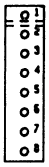


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # HA080475
NETWORK IDENTIFICATION # RN 6

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)



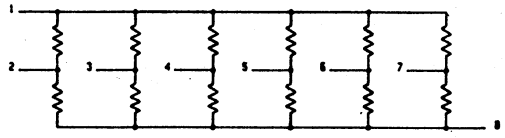
KEY TO LOGIC SYMBOLS	CODE IDENT C	DWG NO 95387500	REV B
		SHEET 111	

TRUTH TABLE

GENERAL OPERATIONAL DESCRIPTION

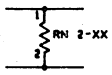
THIS DEVICE IS A SINGLE-IN-LINE RESISTOR NETWORK. IT CONSISTS OF 6 RESISTORS OF ONE VALUE AND 6 RESISTORS OF ANOTHER VALUE. THESE VALUES SHALL BE DETERMINED AS PER DRAWINGS EMPLOYING THIS DEVICE.

NETWORK SCHEMATIC

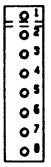


ELEMENT IDENTIFICATION
NETWORK IDENTIFICATION # RN1
VENDOR IDENTIFICATION # 750

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)



REV B

CODE IDENT C

DWG NO 95387500

SHEET 1 12

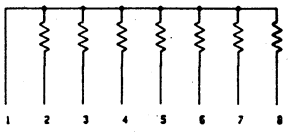
KEY TO LOGIC SYMBOLS

TRUTH TABLE

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A SINGLE-IN-LINE RESISTOR NETWORK. IT CONSISTS OF 8 RESISTORS OF THE SAME VALUES. THESE VALUES SHALL BE DETERMINED AS PER DRAWINGS EMPLOYING THIS DEVICE.

NETWORK SCHEMATIC

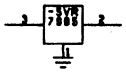


ELEMENT IDENTIFICATION

VENDOR IDENTIFICATION # 750-81-R (VALUE)

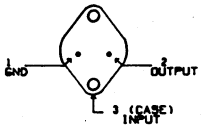
NETWORK IDENTIFICATION # RN 2

SYMBOL/APPLICATION/PINS

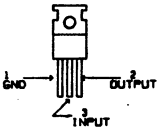


MECHANICAL CONFIGURATION (BOTTOM VIEW)

T03 TYPE



T0220 TYPE



REV	B	
DWG NO	95387500	
SHEET	113	
CODE IDENT	C	

KEY TO LOGIC SYMBOLS

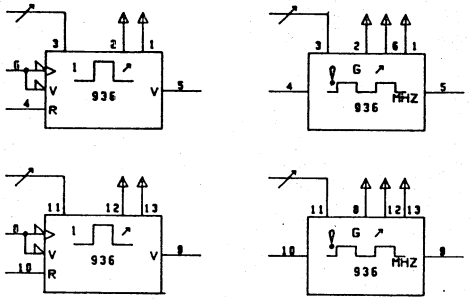
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE (T_J=+25°C)	V_O	-4.8	-5.0	-5.2	VDC
INPUT REGULATION (T_J=+25°C, I_O=100MA)	REG_{IN}				MV
-7.0VDC ≥ V_{IN} ≥ -25VDC			7.0	50	
-8.0VDC ≥ V_{IN} ≥ -12VDC			2.0	25	
(T_J=+25°C, I_O=500MA)					
-7.0VDC ≥ V_{IN} ≥ -25VDC			35	100	
-8.0VDC ≥ V_{IN} ≥ -12VDC			8.0	50	
LOAD REGULATION T_J=+25°C	REG_{LOAD}				MV
5.0MA ≤ I_O ≤ 1.5A			11	100	
250MA ≤ I_O ≤ 750MA			4.0	50	
OUTPUT VOLTAGE -7.0VDC ≥ V_{IN} ≥ -20VDC 5.0MA ≤ I_O ≤ 1.0A, P≤15W		-4.75		-5.25	VDC
QUIESCENT CURRENT (T_J=+25°C)	I_B		4.3	8.0	MA
QUIESCENT CURRENT CHG -7.0VDC ≥ V_{IN} ≥ -25VDC	ΔI_B			1.3	MA
5.0MA ≤ I_O ≤ 1.5A				0.5	
OUTPUT NOISE VOLTAGE (T_A=+25°C) (10HZ ≤ F ≤ 100HZ)	V_N		40		UV
LONG-TERM STABILITY	$\Delta V_O / \Delta T$			20	MV 1.0K HRS
RIPPLE REJECTION I_O=20MA, F=120HZ	RR		70		DB
INPUT-OUTPUT VOLTAGE DIFFERENTIAL I_O=1.0A, T_J=+25°C	$V_{IN}-V_O$		2.0		VDC
AVG. TEM. COEF. OF OUTPUT VOLTAGE I_O=5.0MA, 0°C ≤ T_A ≤+125°C	TCV_O		-1.0		MV/°C

GENERAL OPERATIONAL DESCRIPTION

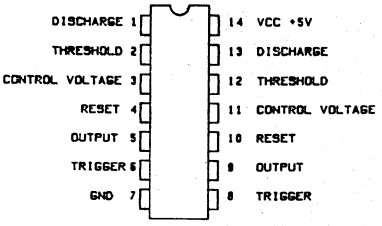
THIS DEVICE IS A THREE-TERMINAL POSITIVE VOLTAGE REGULATORS FOR A WIDE VARIETY OF APPLICATIONS INCLUDING LOCAL, ON-CARD REGULATION. THESE REGULATORS EMPLOY INTERNAL CURRENT LIMITING, THERMAL SHUTDOWN, AND SAFE AREA COMPENSATION-MAKING THEM ESSENTIALLY BLOW-OUT PROOF. WITH ADEQUATE HEATSINKING THEY CAN DELIVER OUTPUT CURRENTS IN EXCESS OF 1.0 AMPERE.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 7905

SYMBOL APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV B

DWG NO 95387500

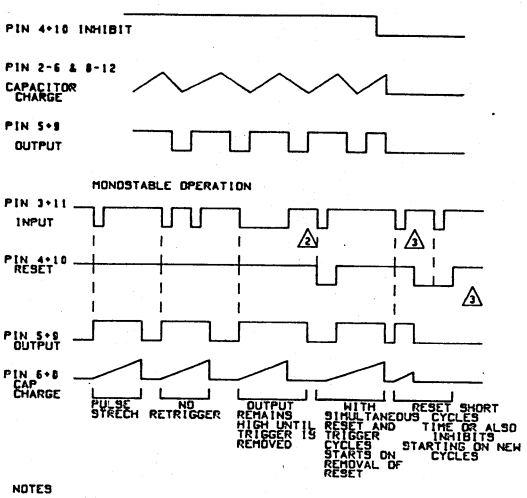
SHEET 114

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

TIMING DIAGRAM



NOTES

1. THIS DEVICE WILL NOT FUNCTION AS A PULSE SHRINKER.
2. THESE EDGES ARE AT THE SAME TIME
3. THERE WILL BE NO TRIGGERING EVEN AFTER REMOVAL OF THE RESET, BECAUSE THE INPUTS OCCURED DURING RESET.

GENERAL OPERATIONAL DESCRIPTION

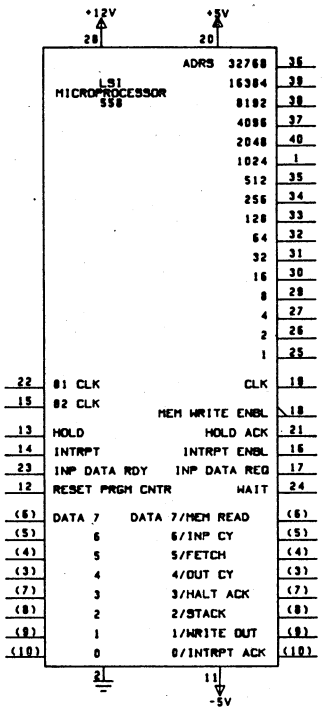
THIS TIMING CIRCUIT IS A HIGHLY STABLE CONTROLLER CAPABLE OF PRODUCING ACCURATE TIME DELAY, OR OSCILLATION. ADDITIONAL TERMINALS ARE PROVIDED FOR TRIGGERING OR RESETTING IF DESIRED. IN THE TIME DELAY MODE OF OPERATION, THE TIME IS PRECISELY CONTROLLED BY ONE EXTERNAL RESISTOR AND CAPACITOR. $T_D = .693\ (R_A + R_B)\ C_X$

$$C_X = \frac{T}{(.693)\ (R_A + R_B)}$$

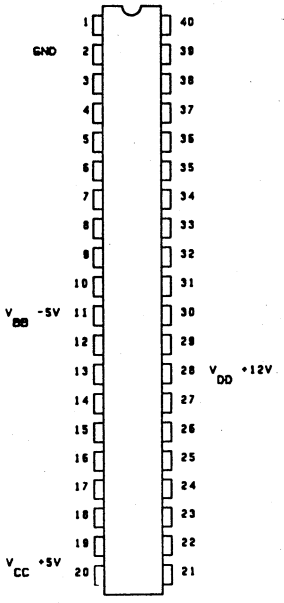
THE CIRCUIT MAY BE TRIGGERED AND RESET ON FALLING WAVE FORMS, AND THE OUTPUT STRUCTURE CAN SOURCE OR SINK UP TO 200MA OR DRIVE TTL CIRCUITS.

ELEMENT IDENTIFICATION # 936
VENDOR IDENTIFICATION # 556

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



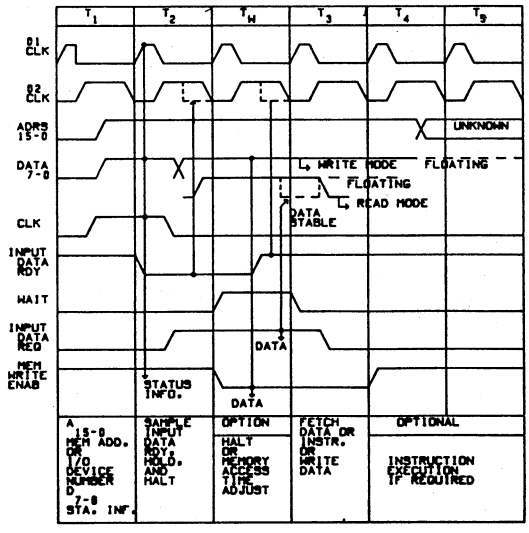
REV C
DWG NO 95387500
SHEET 115
CODE IDENT C
KEY TO LOGIC SYMBOLS

GENERAL OPERATIONAL DESCRIPTION

THE 8080A IS A COMPLETE 8-BIT PARALLEL CENTRAL PROCESSING UNIT WHICH CONTAINS SIX 8-BIT GENERAL PURPOSE WORKING REGISTORS, AN 8-BIT ACCUMULATOR, A 16-BIT STACK POINTER FOR USE WITH AN EXTERNAL STACK, AND FOUR TESTABLE FLAGS. SEPARATE 16 LINE ADDRESS AND 8-LINE BI-DIRECTIONAL DATA BUSSES ARE USED TO INTERFACE TO MEMORY AND I/O.

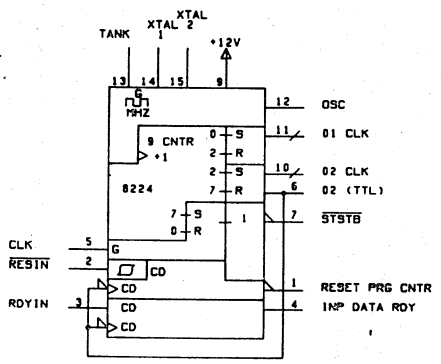
TIMING DIAGRAM

BASIC 8080A INSTRUCTION CYCLE

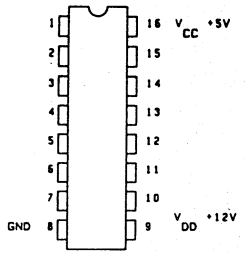


ELEMENT IDENTIFICATION # 558
VENDOR INDETIFICATION # 8080A, 8080A

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



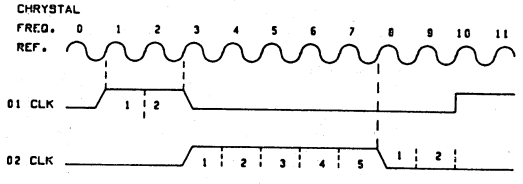
$\overline{RESIN}$	RESET INPUT
RESET	RESET OUTPUT
PRG CNTR RDYIN	READY INPUT
SYNC	SYNC INPUT
$\overline{STSTB}$	STATUS STB (ACTIVE LOW)
01 CLK 02 CLK	8080 CLOCKS

XTAL 1 XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE CRYSTAL
OSC	OSCILLATOR OUTPUT
02 (TTL)	02 CLK (TTL LEVEL)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

GENERAL OPERATIONAL DESCRIPTION

THE 8224 IS A CRYSTAL CONTROLLED CLOCK GENERATOR/DRIVER FOR THE 8080A CPU. ALSO INCLUDED ARE CIRCUITS TO PROVIDE POWER-UP RESET, STATUS STROBE AND SYNCHRONIZATION OF READY.

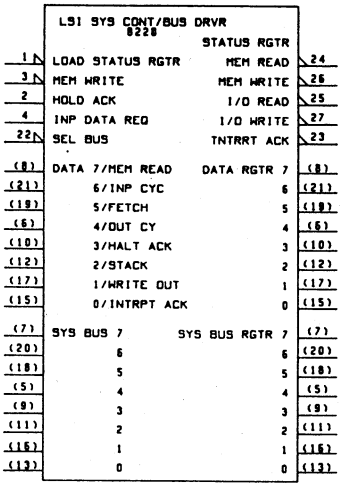
TIMING DIAGRAM



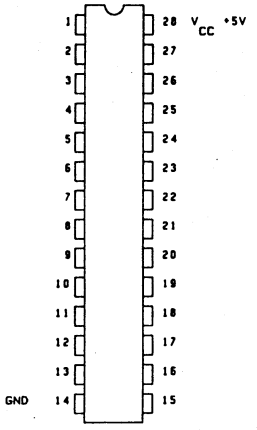
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 8224

REV C
DWG NO 95387500
SHEET 116
CODE IDENT C
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



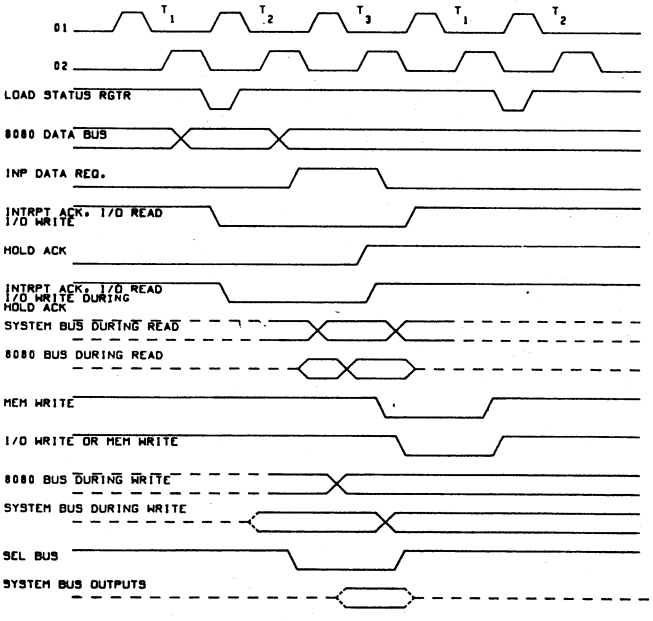
MECHANICAL CONFIGURATION (TOP VIEW)



REV C
DWG NO 95387500
SHEET 117
CODE IDENT C
KEY TO LOGIC SYMBOLS

TRUTH TABLE

TIMING DIAGRAM

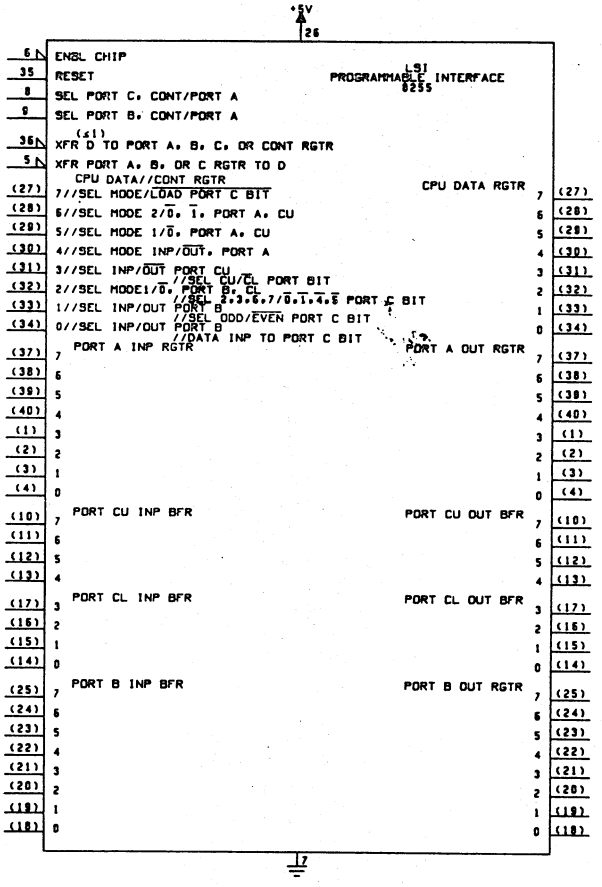


GENERAL OPERATIONAL DESCRIPTION

THE 8228 IS A SYSTEM CONTROLLER AND BUS DRIVER WHICH GENERATES CONTROL SIGNALS REQUIRED TO INTERFACE RAM, ROM, AND I/O COMPONENTS TO THE 8080A CPU. THE CONTROL SIGNALS ARE DERIVED FROM THE 8080A 'STATUS' INFORMATION ON THE DATA BUS WHICH INDICATES THE TYPE OF ACTIVITY THAT WILL OCCUR DURING THAT CYCLE.

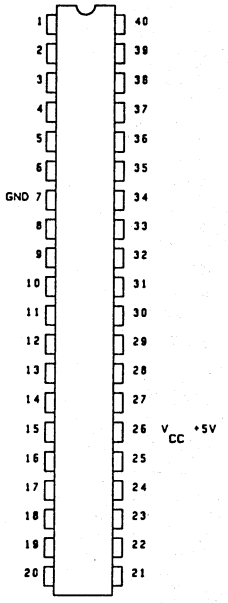
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 8228

SYMBOL/APPLICATION/PINS



TIMING DIAGRAM

MECHANICAL CONFIGURATION (TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THE 8255 IS A GENERAL PURPOSE PROGRAMMABLE I/O DEVICE USED WITH THE 8080A CPU. IT HAS 24 I/O PINS WHICH MAY BE INDIVIDUALLY PROGRAMMED IN TWO GROUPS OF TWELVE AND USED IN THREE MAJOR MODES OF OPERATION.

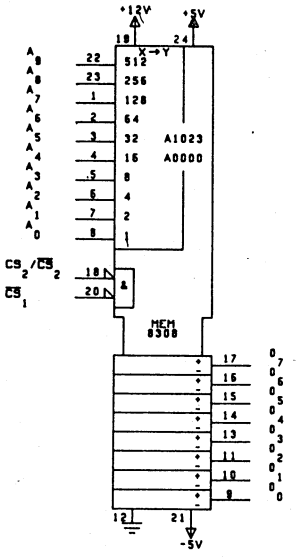
- MODE 0- EACH GROUP OF TWELVE I/O PINS MAY BE PROGRAMMED IN SETS OF 4 TO BE EITHER INPUT OR OUTPUT
- MODE 1- EACH GROUP MAY BE PROGRAMMED TO HAVE 8 LINES OF INPUT OR OUTPUT OF THE REMAINING 4 PINS IN EACH GROUP, THREE ARE USED FOR HANDSHAKING, AND INTERRUPT CONTROL SIGNALS.
- MODE 2- A BI-DIRECTIONAL BUS WHICH USES 8 LINES (BORROWING ONE LINE FROM THE OTHER GROUP) FOR HANDSHAKING.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 8255

KEY TO LOGIC SYMBOLS

CODE IDENT C | DWG NO 95387500 | REV C | SHEET 118

SYMBOL/APPLICATION/PINS

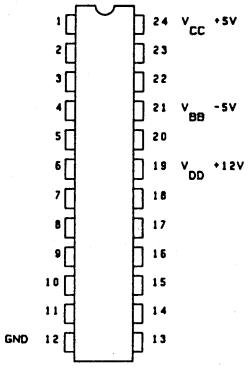


A_0-A_9 ADDRESS INPUT

O_1-O_8 DATA OUTPUT

$\overline{CS}_1$,CS_2 CHIP SELECT INPUTS

MECHANICAL CONFIGURATION (TOP VIEW)



REV	C
DWG NO	95387500
CODE IDENT	C
SHEET 118	

KEY TO LOGIC SYMBOLS

TRUTH TABLE

TIMING DIAGRAM

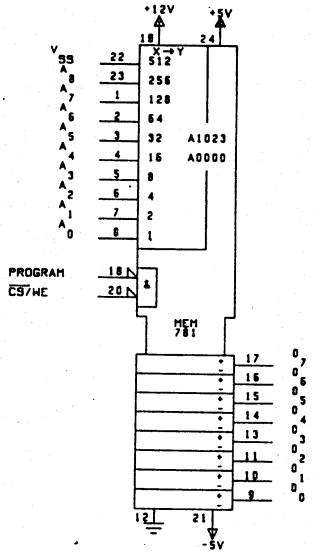
GENERAL OPERATIONAL DESCRIPTION

THE 8308 IS 8192 BIT STATIC-MOS MASK PROGRAMMABLE READ ONLY MEMORY ORGANIZED AS 1024 WORDS BY 8 BITS. THE CIRCUIT FEATURES TWO CHIP SELECTS, $\overline{CS1}$ WHICH IS NEGATIVE TRUE, AND CS2/$\overline{CS2}$ WHICH CAN BE PROGRAMMED EITHER NEGATIVE OR POSITIVE TRUE AT THE MASK LEVEL.

ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 8308

SYMBOL/APPLICATION/PINS



A_0-A_9 ADDRESS INPUTS

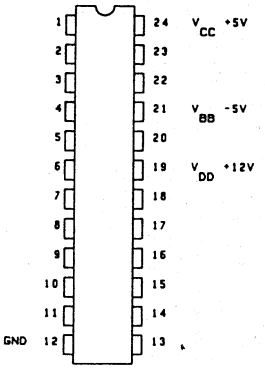
O_1-O_8 DATA OUTPUTS

$\overline{CS}/WE$ CHIP SELECT/WRITE ENABLE INPUT

TRUTH TABLE

TIMING DIAGRAM

MECHANICAL CONFIGURATION (TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

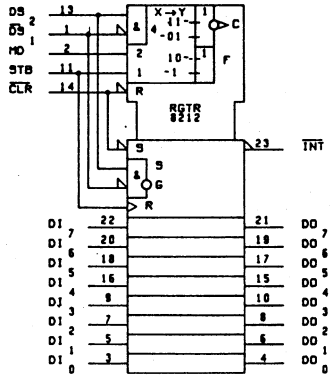
THE 8708 IS A 8192 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE 'READ ONLY MEMORY' ORGANIZED AS 1024 WORDS BY 8 BITS. THE CIRCUIT PACKAGE FEATURES A TRANSPARENT LID WHICH ALLOWS THE USER TO EXPOSE THE CHIP TO ULTRAVIOLET LIGHT TO ERASE THE BIT PATTERN. PROGRAMMING IS ACCOMPLISHED BY USING A SPECIAL PROM PROGRAMMING DEVICE.

ELEMENT IDENTIFICATION # 781
VENDOR IDENTIFICATION # 8708

KEY TO LOGIC SYMBOLS

CODE IDENT C | DWG NO 95387500 | REV C | SHEET 120

SYMBOL/APPLICATION/PINS



TRUTH TABLE

STB	MD	$(\overline{DS}_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	3 - STATE
1	0	0	3 - STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ - RESET DATA LATCH
SETS SR FF
(NO EFFECT ON OUTPUT BUFFER)

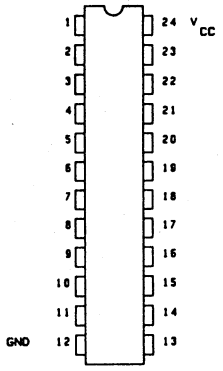
CLR	$(\overline{DS}_1 \cdot DS_2)$	STB	*SR	INT
0	0	0	1	1
0	1	0	1	0
1	1	↓	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↓	1	0

* INTERNAL SR FLIP-FLOP

DI_0-DI_8 DATA IN
DO_0-DO_8 DATA OUT
$\overline{DS}_1^0$-DS_2^8 DEVICE SELECT
MD_1^2 MODE
STB STROBE
$\overline{INT}$ INTERRUPT (ACTIVE LOW)
$\overline{CLR}$ CLEAR (ACTIVE LOW)

TIMING DIAGRAM

MECHANICAL CONFIGURATION (TOP VIEW)



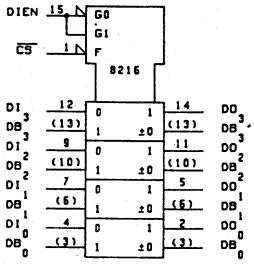
GENERAL OPERATIONAL DESCRIPTION

THE 8212 IS AN INPUT/OUTPUT PORT CONTAINING AN 8-BIT LATCH WITH 3 STATE BUFFERS ALONG WITH CONTROL AND DEVICE SELECTION LOGIC. ALSO INCLUDED IS A SERVICE REQUEST (SR) FF WHICH CAN BE USED FOR THE GENERATION AND CONTROL OF INTERRUPTS TO A CPU. THE DEVICE IS MULTIMODE IN NATURE AS IT CAN BE USED TO IMPLEMENT LATCHES, GATED BUFFERS OR MULTIPLEXERS.

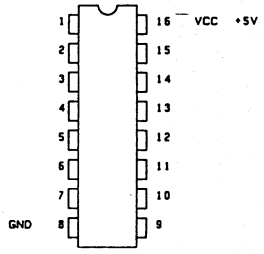
ELEMENT IDENTIFICATION 8
VENDOR IDENTIFICATION 8 8212

KEY TO LOGIC SYMBOLS
CODE IDENT C
DWG NO 95387500
REV C
SHEET 121

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE

$\overline{DIEN}$	$\overline{CS}$	
0	0	DI → DB
1	0	DB → DO
0	1	HIGH IMPEDANCE
1	1	

DO_0-BD_3 DATA BUS BI-DIRECTIONAL

DI_0-DI_3 DATA INPUT

DO_0-DO_3 DATA OUTPUT

$\overline{DIEN}$ DATA IN ENABLE DIRECTION CONTROL

$\overline{CS}$ CHIP SELECT

GENERAL OPERATIONAL DESCRIPTION

THE 8216 IS A 4-BIT BI-DIRECTIONAL DRIVER/BUFFER

TIMING DIAGRAM

ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 8216

KEY TO LOGIC SYMBOLS

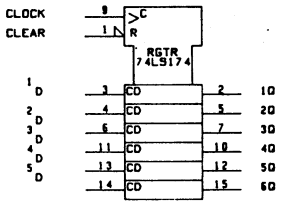
CODE IDENT C

DWG NO 95387500

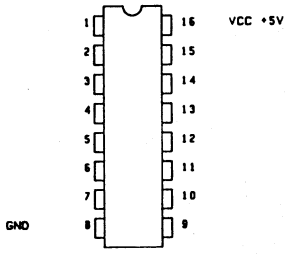
REV C

SHEET 122

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV B

DWG NO 95387500

SHEET 123

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVANT
↑ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.

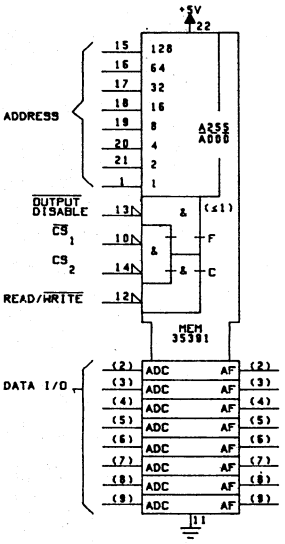
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

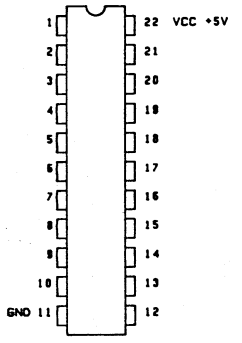
THIS MONOLITHIC POSITIVE-EDGE-TRIGGERED FLIP-FLOP UTILIZES TTL CIRCUITRY TO IMPLEMENT D TYPE FLIP-FLOP LOGIC.
INFORMATION AT THE D INPUT MEETING THE SETUP TIME REQUIREMENTS IS TRANSFERRED TO THE Q OUTPUTS ON THE POSITIVE-GOING EDGE OF THE CLOCK PULSE. CLOCK TRIGGERING OCCURS AT A PARTICULAR VOLTAGE LEVEL AND IS NOT DIRECTLY RELATED TO THE TRANSITION TIME OF THE POSITIVE-GOING PULSE. WHEN THE CLOCK INPUT IS AT EITHER THE HIGH OR LOW LEVEL, THE D INPUT SIGNAL HAS NO EFFECT AT THE OUTPUT. THIS DEVICE FEATURES SIX FLIP-FLOPS WITH A COMMON DIRECT CLEAR.

ELEMENT IDENTIFICATION 8
VENDOR IDENTIFICATION #74LS174

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B		
DWG NO	C	95387500	
CODE IDENT			SHEET 124

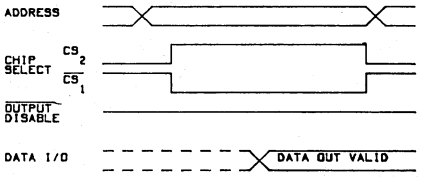
KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC

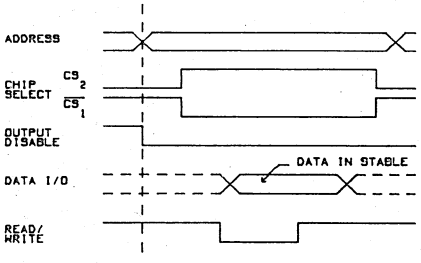
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A 256 WORD BY 8 BIT STATIC RANDOM ACCESS MEMORY. THE DATA IS READ OUT NONDESTRUCTIVELY AND HAS THE SAME LOGIC SENSE AS THE INPUT DATA. THE MEMORY IS FABRICATED WITH N-CHANNEL SILICON GATE TECHNOLOGY AND HAS TTL COMPATIBLE INPUTS AND OUTPUTS. THE OUTPUTS ARE THREE-STATE TO ALLOW OR-TIE CAPABILITY.

TIMING DIAGRAM
READ CYCLE

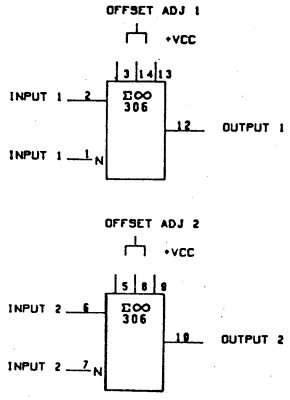


TIMING DIAGRAM
WRITE CYCLE

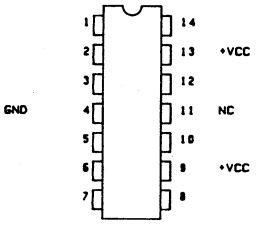


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #35381DC

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	B
DWG NO	95387500
SHEET	125
CODE IDENT	C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

THE 747 IS A PAIR OF HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS. THEY ARE INTENDED FOR A WIDE RANGE OF ANALOG APPLICATIONS. HIGH COMMON MODE VOLTAGE RANGE AND ABSENCE OF LATCH-UP MAKE THE 747 IDEAL FOR USE AS A VOLTAGE FOLLOWER. THE HIGH GAIN AND WIDE RANGE OF OPERATING VOLTAGE PROVIDES SUPERIOR PERFORMANCE IN INTEGRATOR, SUMMING AMPLIFIER, AND GENERAL FEEDBACK APPLICATIONS. THE 747 IS SHORT CIRCUIT PROTECTED AND REQUIRES NO EXTERNAL COMPONENTS FOR FREQUENCY COMPENSATION. THE INTERNAL 6DB/OCTAVE ROLL-OFF INSURES STABILITY IN CLOSED LOOP APPLICATIONS.

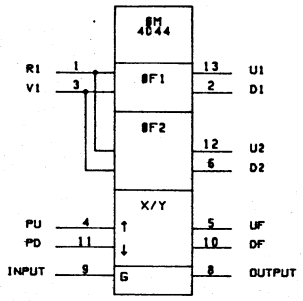
TIMING DIAGRAM

N/A

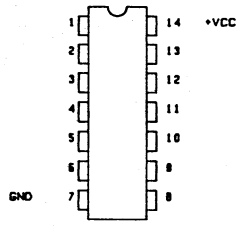
ELEMENT IDENTIFICATION #306

VENDOR IDENTIFICATION # MC1747
MC1747C
UA747
LM747
UA747C
LM747C
SN52747Z
NS747A

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE

THIS IS NOT STRICTLY A FUNCTIONAL TRUTH TABLE; I.E., IT DOES NOT SHOW ALL POSSIBLE MODES OF OPERATION. IT IS USEFUL FOR DC TESTING.

INPUT STATE	INPUT			OUTPUT		
	R1	V1	U1	D1	U2	D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

1. X-INDICATES OUTPUT STATE UNKNOWN.
2. U1 AND D1 OUTPUTS ARE SEQUENTIAL; I.E. THEY MUST BE SEQUENCED IN ORDER SHOWN.
3. U2 AND D2 OUTPUTS ARE COMBINATIONAL; I.E., THEY NEED ONLY INPUTS SHOWN TO OBTAIN OUTPUTS.

TIMING DIAGRAM

N/A

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE CONTAINS TWO DIGITAL PHASE DETECTORS AND A CHARGE PUMP CIRCUIT WHICH CONVERTS MTTL INPUTS TO A DC VOLTAGE LEVEL FOR USE IN FREQUENCY DISCRIMINATION AND PHASE-LOCKED-LOOP APPLICATIONS.

THE TWO PHASE DETECTORS HAVE COMMON INPUTS. PHASE FREQUENCY DETECTOR 1 IS LOCKED IN (INDICATED BY BOTH OUTPUTS HIGH) WHEN THE NEGATIVE TRANSITIONS OF THE VARIABLE INPUT (V1) AND REFERENCE INPUT (R1) ARE EQUAL IN FREQUENCY AND PHASE. IF THE VARIABLE INPUT IS LOWER IN FREQUENCY OR LAGS IN PHASE, THE U1 (UP) OUTPUT GOES LOW. CONVERSELY THE D1 (DOWN) OUTPUT GOES LOW WHEN THE VARIABLE INPUT IS HIGHER IN FREQUENCY OR LEADS THE REFERENCE INPUT IN PHASE. IT IS IMPORTANT TO NOTE THAT THE DUTY CYCLES OF THE VARIABLE INPUT AND THE REFERENCE INPUT ARE NOT IMPORTANT SINCE NEGATIVE TRANSITIONS CONTROL SYSTEM OPERATION.

PHASE DETECTOR 2, ON THE OTHER HAND, IS LOCKED IN WHEN VARIABLE INPUT PHASE LAGS THE REFERENCE PHASE BY 90° (INDICATED BY THE U2 AND D2 OUTPUTS ALTERNATELY GOING LOW WITH EQUAL PULSE WIDTHS). IF THE VARIABLE INPUT PHASE LAGS BY MORE THAN 90°, U2 WILL REMAIN LOW LONGER THAN D2, AND, CONVERSELY, IF THE VARIABLE INPUT PHASE LAGS THE REFERENCE PHASE BY LESS 90°, D2 REMAINS LOW LONGER. IN THIS PHASE DETECTOR THE VARIABLE INPUT AND THE REFERENCE MUST HAVE 50% DUTY CYCLES.

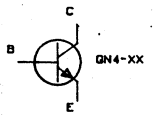
THE CHARGE PUMP ACCEPTS THE PHASE DETECTOR (U1 OR U2 APPLIED TO PU, AND D1 OR D2 APPLIED TO PD) AND CONVERTS THEM TO FIXED AMPLITUDE POSITIVE AND NEGATIVE PULSES AT THE UF AND DF OUTPUTS RESPECTIVELY. THESE PULSES ARE APPLIED TO A LAG-LEAD ACTIVE FILTER, WHICH INCORPORATES EXTERNAL COMPONENTS, AS WELL AS THE AMPLIFIER PROVIDED IN THE MC4344/4044 CIRCUIT. THE FILTER PROVIDES A DC VOLTAGE PROPORTIONATELY TO THE PHASE ERROR.

ELEMENT IDENTIFICATION # 4044
VENDOR IDENTIFICATION # MC4044P
MC4044L

KEY TO LOGIC SYMBOLS

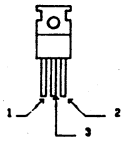
CODE IDENT C | DWG NO 95387500 | REV B | SHEET 126

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)

TO-220 TYPE



1. BASE
2. EMITTER
3. (CASE) COLLECTOR

KEY TO LOGIC SYMBOLS	CODE IDENT C	DWG NO 95387500	SHEET 127	REV D

TRUTH TABLE

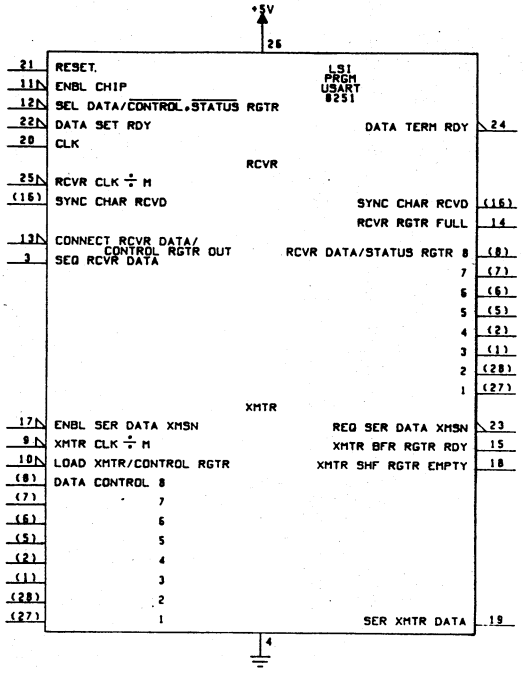
GENERAL OPERATIONAL DESRIPTION

DARLINGTON 6 AMPERE COMPLEMENTARY SILICON POWER TRANSISTOR IS DESIGNED FOR GENERAL PURPOSE AMPLIFIER AND LOW SPEED SWITCHING APPLICATIONS. THIS DEVICE HAS HIGH CURRENT GAIN WITH COLLECTOR EMITTER SUSTAINING VOLTAGE. IT IS A MONOLITHIC CONSTRUCTION WITH BUILT IN BASE-EMITTER SHUNT RESISTORS.

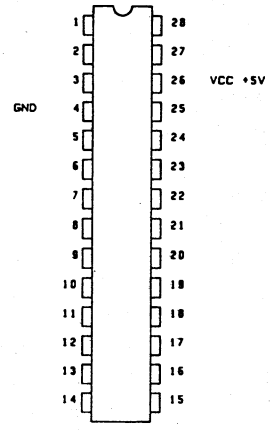
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 95358400 & 95358401
NETWORK IDENTIFICATION # QN4

SYMBOLS/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV E
DWG NO 95387500
SHEET 120
CODE IDENT C
KEY TO LOGIC SYMBOLS

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A UNIVERSAL SYNCHRONOUS/ASYNCHRONOUS RECEIVER/TRANSMITTER (USART) DESIGNED FOR DATA COMMUNICATIONS IN MICROPROCESSOR SYSTEMS. IT IS USED AS A PERIPHERAL DEVICE AND IS PROGRAMMED BY THE CPU. IT CAN ACCEPT PARALLEL DATA FROM THE CPU AND CONVERT IT TO SERIAL FORMAT FOR TRANSMISSION. SIMULTANEOUSLY IT CAN RECEIVE SERIAL DATA AND CONVERT IT TO PARALLEL FORMAT FOR THE CPU. IN EITHER STATE OF OPERATION THIS DEVICE WILL DELETE OR INSERT BITS OR CHARACTERS THAT ARE FUNCTIONALLY UNIQUE TO THE COMMUNICATION TECHNIQUE. VARIOUS STATUS SIGNALS ARE SENT TO THE CPU AT PREDETERMINED TIMES OR ON CPU COMMAND.

TRUTH TABLE

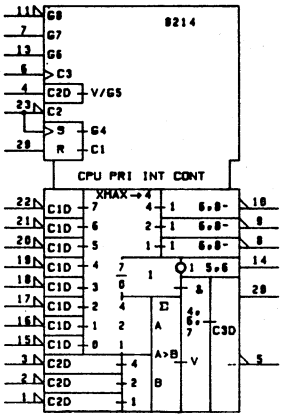
NA

TIMING DIAGRAM

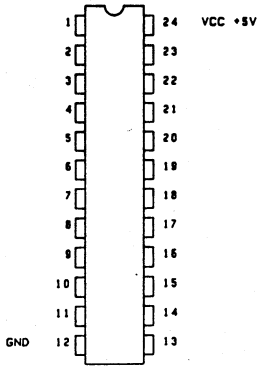
NA

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 8251

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS

CODE IDENT C DWG NO 95387500 REV E

SHEET 128

TRUTH TABLE

NA

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS AN EIGHT LEVEL PRIORITY INTERRURT CONTROL UNIT DESIGNED FOR USE WITH MICROPROCESSOR SYSTEMS. IT CAN ACCEPT EIGHT REQUESTING LEVELS; DETERMINE THE HIGHEST PRIORITY, COMPARE THIS PRIORITY TO A SOFTWARE CONTROLLED CURRENT STATUS REGISTER AND ISSUE AN INTERRUPT TO THE SYSTEM ALONG WITH VECTOR INFORMATION TO IDENTIFY THE SERVICE ROUTINE. IT PROVIDES FOR CASCADING TWO OR MORE CHIPS TO ALLOW EXPANSION TO MORE THAN EIGHT LEVELS OF INTERRUPT BY SPECIAL INPUTS AND OPEN COLLECTOR OUTPUTS.

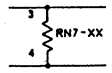
TIMING DIAGRAM

NA

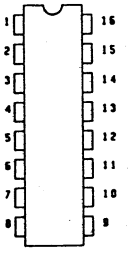
ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 8214

SYMBOLS/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS	CODE IDENT	DWG NO	REV
	C	95387500	F
		SHEET 130	

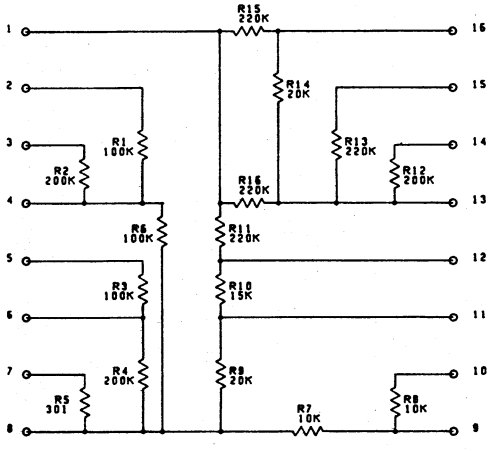
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

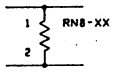
THIS DEVICE IS A DUAL-IN-LINE RESISTOR NETWORK.

CIRCUIT DIAGRAM

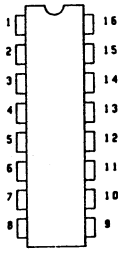


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 44671763
NETWORK IDENTIFICATION # RN7

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)

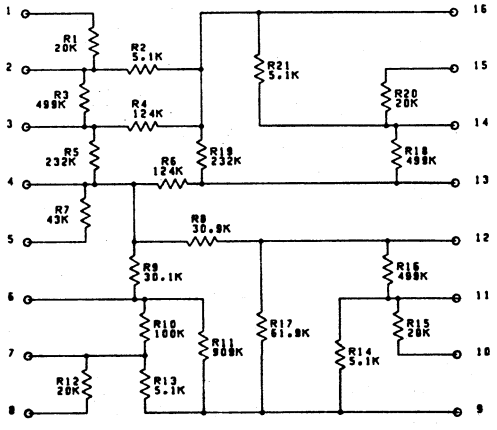


KEY TO LOGIC SYMBOLS	CODE IDENT C	DWG NO 95387500	REV F
		SHEET 131	

GENERAL OPERATIONAL DESCRIPTION

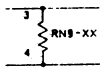
THIS DEVICE IA A DUAL-IN-LINE RESISTOR NETWORK.

CIRCUIT DIAGRAM

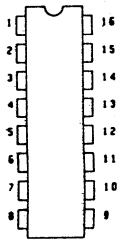


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 44671762
NETWORK IDENTIFICATION # RN8

SYMBOLS/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV F
CODE IDENT C
DWG NO 95387500
SHEET 132

KEY TO LOGIC SYMBOLS

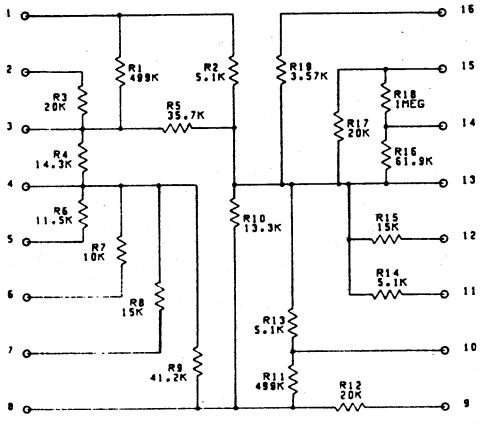
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL-IN-LINE RESISTOR NETWORK.

TRUTH TABLE

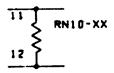
N/A

CIRCUT DIAGRAM

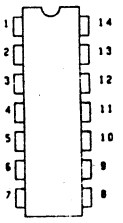


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #44671761
NETWORK IDENTIFICATION #RN9

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV F

CODE IDENT C

DWG NO 95387500

SHEET 133

KEY TO LOGIC SYMBOLS

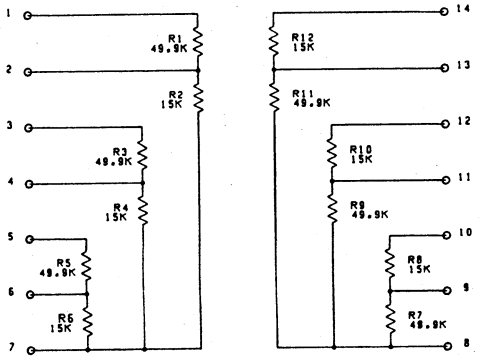
TRUTH TABLE

NA

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL-IN-LINE RESISTOR NETWORK

CIRCUT DIAGRAM

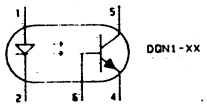


ELEMENT IDENTIFICATION #

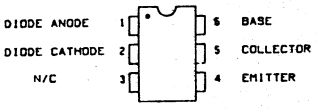
VENDOR IDENTIFICATION #44671764

NETWORK IDENTIFICATION #RN10

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



		REV	F
CODE IDENT	C	DWG NO	9538'7500
		SHEET	134

KEY TO LOGIC SYMBOLS

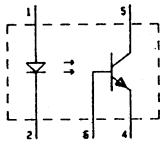
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

THIS PHOTON-COUPLED ISOLATOR IS CHARACTERIZED FOR A LOW V_{CE}(SAT) UP TO 0.5MA COLLECTOR CURRENT WITH A FORWARD LED CURRENT OF 20MA. THIS OPTICAL COUPLER IS GENERALLY USED AS AN ISOLATING SWITCH BETWEEN TWO ELECTRICAL CIRCUITS. WHEN NO CURRENT FLOWS THRU THE LED THE OUTPUT TRANSISTOR IS OFF. WHEN CURRENT FLOWS THRU THE LED, PHOTONS ARE GENERATED SUPPLYING BASE DRIVE TO THE OUTPUT TRANSISTOR- IN TURN ABLE TO SINK COLLECTOR CURRENT (OR SOURCE EMITTER CURRENT)

CIRCUIT DIAGRAM

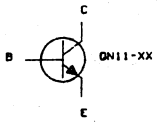


ELEMENT IDENTIFICATION #

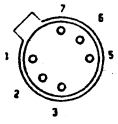
VENDOR IDENTIFICATION # H11A5 & SOC140

NETWORK IDENTIFICATION # DQN1

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)



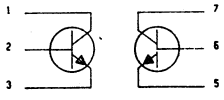
CODE IDENT	C	DWG NO 95387500	REV F
KEY TO LOGIC SYMBOLS		SHEET 135	

TRUTH TABLE

GENERAL OPERATIONAL DESCRIPTION

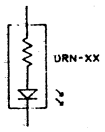
DUAL NPN SILICON LOW CURRENT AMPLIFIER TRANSISTORS FOR DIFFERENTIAL AMPLIFIER APPLICATIONS WHERE TEMPERATURE TRACKING AND SPECIFIED MATCHING OF BASE TO EMITTER VOLTAGE IS REQUIRED.

CIRCUIT DIAGRAM

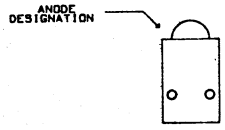


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # MD8002
NETWORK IDENTIFICATION # QN11

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)



REV F

DWG NO 95387500

SHEET 136

CODE IDENT C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

GENERAL OPERATIONAL DESCRIPTION

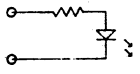
THIS DEVICE IS A LIGHT EMITTING DIODE WITH INTERNAL CURRENT LIMITING RESISTOR DESIGNED TO OPERATE FROM A NOMINAL 5V SUPPLY. IT IS USED AS AN INDICATOR FOR VISUAL DISPLAY.

ELEMENT IDENTIFICATION #

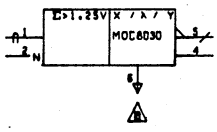
VENDOR IDENTIFICATION # 44670863

NETWORK IDENTIFICATION # DRN 1

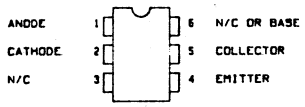
CIRCUIT DIAGRAM



SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV.	F
DWG. NO	95387500
SHEET	137

KEY TO LOGIC SYMBOLS

TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

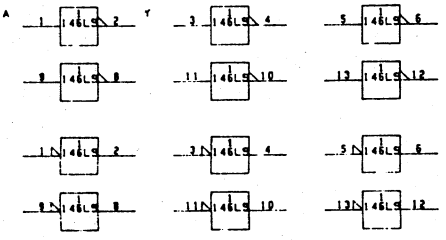
THIS DEVICE CONTAINS A GALLIUM ARSENID LED OPTICALLY COUPLED TO A SILICON PHOTO TRANSISTOR DESIGNED FOR APPLICATIONS REQUIRING ELECTRICAL ISOLATION. HIGH BREAKDOWN VOLTAGE.

TIMING DIAGRAM

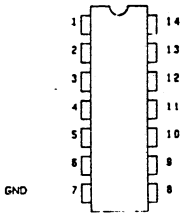
N/A

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #MOC8030

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS

CODE IDENT C | DWG NO 95387500 | REV F | SHEET 138

TRUTH TABLE

POS LOGIC $Y=\overline{A}$

A	Y
0	1
1	0

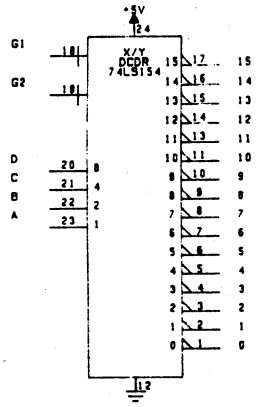
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TTL HEX INVERTER.

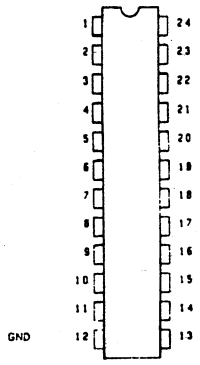
TIMING DIAGRAM

ELEMENT IDENTIFICATION #146LS
VENDOR IDENTIFICATION #74LS04

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	F		
DWG. NO	95387500		
CODE IDENT	C	SHEET 139	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

INPUT					OUTPUT														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

NOTES
1. H = HIGH
2. L = LOW
3. X = IRRELEVANT

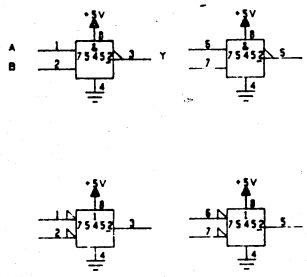
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

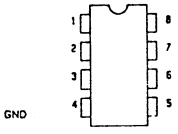
THIS MONOLITHIC 4-LINE-TO-16-LINE DECODER UTILIZES TTL CIRCUITRY TO DECODE FOUR BINARY-CODED INPUTS INTO ONE OF SIXTEEN MUTUALLY EXCLUSIVE OUTPUTS WHEN BOTH THE STROBE INPUTS G1 AND G2 ARE LOW. THE DEMULTIPLEXING FUNCTION IS PERFORMED BY USING THE 4 INPUT LINES TO ADDRESS THE OUTPUT LINE. PASSING DATA FROM ONE OF THE STROBE INPUTS WITH THE OTHER STROBE INPUT LOW. WHEN EITHER STROBE INPUT IS HIGH, ALL OUTPUTS ARE HIGH.

ELEMENT IDENTIFICATION #167LS
VENDOR IDENTIFICATION #74LS154

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	F
DWG NO	95387500
CODE IDENT	C
SHEET 140	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC Y=A•B

A	B	Y	
0	0	1	OFF STATE
0	1	1	OFF STATE
1	0	1	OFF STATE
1	1	0	ON STATE

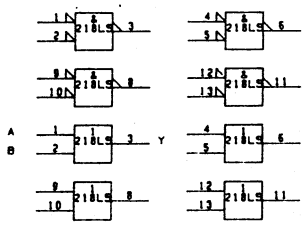
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL PERIPHERAL POSITIVE NAND DRIVER (ASSUMING POSITIVE LOGIC) WITH THE OUTPUT OF THE LOGIC GATES INTERNALLY CONNECTED TO THE BASES OF THE N-P-N OUTPUT TRANSISTORS. THE CIRCUIT OUTPUT ARE OPEN COLLECTOR OUTPUTS.

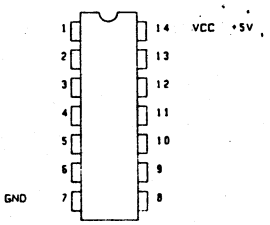
TIMING DIAGRAM

ELEMENT IDENTIFICATION #.
VENDOR IDENTIFICATION #75452

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



CODE IDENT	C	DWG NO	95387500	REV	F
		SHEET 141			

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC Y=A•B

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

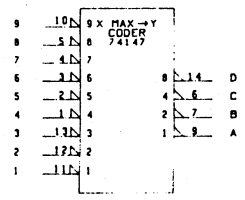
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE 2 INPUT TTL POSITIVE OR GATE.

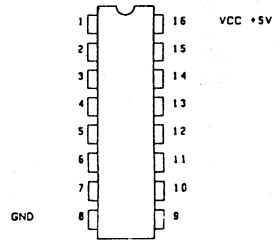
TIMING DIAGRAM

ELEMENT IDENTIFICATION #218LS
VENDOR IDENTIFICATION #74LS32

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV F
DWG NO 95387500
CODE IDENT C
SHEET 142
KEY TO LOGIC SYMBOLS

TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH LOGIC LEVEL
L = LOW LOGIC LEVEL
X = IRRELEVENT

TIMING DIAGRAM

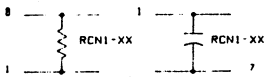
N/A

GENERAL OPERATIONAL DISCRIPTION

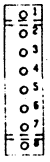
THIS DEVICE IS A PRIORITY ENCODER. IT DECODES ITS INPUT LINES TO ENSURE THAT ONLY THE HIGHEST ORDER DATA LINE IS ENCODED. THE IMPLIED ZERO CONDITION IS ENCODED WHEN ALL NINE DATA LINES ARE AT A HIGH LOGIC LEVEL. THE NINE DATA LINES ARE ENCODED TO FOUR-LINE (8-4-2-1) BCD.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #74147

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (BOTTOM VIEW)



REV	F
DWG NO	5538750
SHEET 143	
CODE IDENT	C

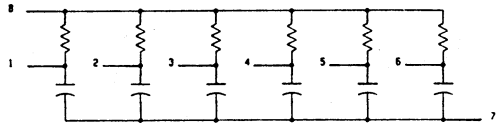
KEY TO LOGIC SYMBOLS

TRUTH TABLE

GENERAL OPERATIONAL DESCRIPTION

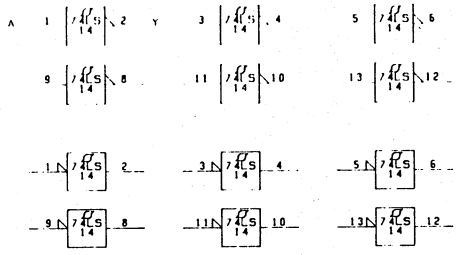
THIS DEVICE IS A SINGLE-IN-LINE RESISTOR CAPACITOR NETWORK. IT CONSISTS OF 6 RESISTORS OF ONE VALUE AND 6 CAPACITORS OF ONE VALUE. THESE VALUES SHALL BE DETERMINED AS PER DRAWING EMPLOYING THIS DEVICE.

NETWORK SCHEMATIC

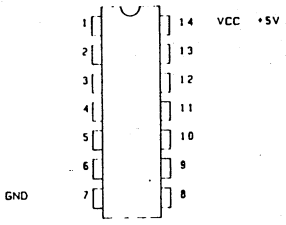


ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #750
NETWORK IDENTIFICATION #RCN1

SYMBOL APPLICATION PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	F
DWG NO	95387500
CODE IDENT	C
SHEET 144	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS LOGIC $Y=\overline{A}$

A	Y
1	0
0	1

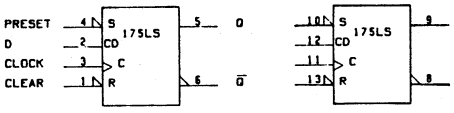
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A TTL HEX SCHMITT-TRIGGER
INVERTER WITH TOTEM-POLE OUTPUTS.
POSITIVE THRESHOLD=1.5V MIN.
NEGATIVE THRESHOLD=1.1V MAX.

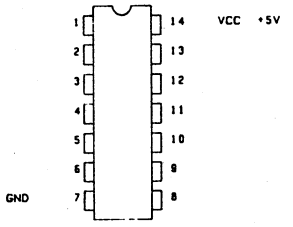
TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #74LS14

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	F
DWG NO	95387500
CODE IDENT	C
SHEET 145	

KEY TO LOGIC SYMBOLS

TRUTH TABLE
POS-LOGIC

T_N	T_{N+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES

1. T_N = BIT TIME BEFORE CLOCK PULSE.
2. T_{N+1} = BIT TIME AFTER CLOCK PULSE.
3. A LOW INPUT TO PRESET SETS Q TO LOGICAL 1.
   A LOW INPUT TO CLEAR SETS Q TO LOGICAL 0.
   THE PRESET AND CLEAR ARE INDEPENDENT OF THE CLOCK.

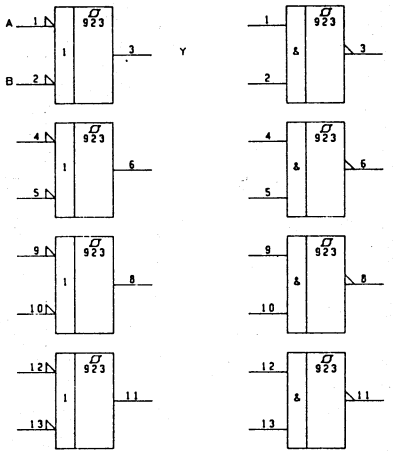
TIMING DIAGRAM

GENERAL OPERATIONAL DESCRIPTION

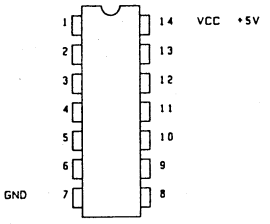
THESE MONOLITIC, DUAL, D-TYPE, EDGE TRIGGERED FLIP-FLOPS FEATURE DIRECT CLEAR AND PRESET INPUTS AND COMPLEMENTARY Q AND $\overline{Q}$ OUTPUTS. INPUT INFORMATION IS TRANSFERRED. TO THE OUTPUTS ON THE POSITIVE EDGE OF THE CLOCK PULSE. CLOCK TRIGGERING OCCURS AT A VOLTAGE LEVEL OF THE CLOCK PULSE AND IS NOT DIRECTLY RELATED TO THE TRANSITION TIME OF THE POSITIVE GOING PULSE. AFTER THE CLOCK INPUT THRESHOLD VOLTAGE HAS BEEN PASSED, THE DATA INPUT (D) IS LOCKED OUT.

ELEMENT IDENTIFICATION #175LS
VENDOR IDENTIFICATION #74LS74

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



KEY TO LOGIC SYMBOLS

CODE IDENT	DWG NO	REV
C	95387500	F

SHEET 146

TRUTH TABLE
POS LOGIC Y=A•B

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

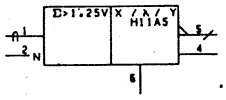
GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A QUADRUPLE 2 INPUT TTL NAND SCHMIDT TRIGGER.

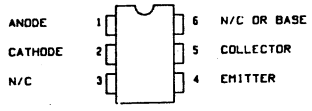
TIMING DIAGRAM

ELEMENT IDENTIFICATION #923
VENDOR IDENTIFICATION #74132

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV G
DWG NO 95387500
SHEET 147
CODE IDENT C
KEY TO LOGIC SYMBOLS

TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE CONTAINS A GALLIUM ARSENIDE L.E.D. OPTICALLY COUPLED TO A SILICON PHOTO TRANSISTOR DESIGNED FOR APPLICATIONS REQUIRING ELECTRICAL ISOLATION. HIGH BREAKDOWN VOLTAGE.

WHEN CURRENT IS INJECTED INTO THE LIGHT EMITTING DIODE TERMINAL, THE PHOTO TRANSISTOR IS CAUSED TO CONDUCT WITH A GUARANTEED VCE (MAX) OF 0.25 VOLTS AT 0.5 MA COLLECTOR CURRENT WITH 20 MA INTO THE L.E.D.

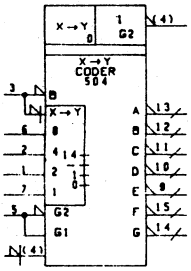
TIMING DIAGRAM

N/A

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # H11A5 , 90C149 ⚠1

⚠1 THIS DEVICE IS PROGRAMED FOR CPI, UNDER PART NO. 44670674.

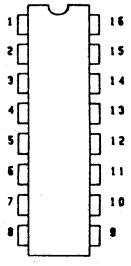
SYMBOL/APPLICATION/PINS



PIN 4 IS A BLANKING INPUT
AND A RIPPLE BLANKING OUTPUT

PIN 5 IS A RIPPLE BLANKING INPUT

MECHANICAL CONFIGURATION (TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE PROVIDES BCD INPUT TO 7 SEGMENTS DRIVER DECODING. THIS DEVICE FEATURES A BLANKING INPUT (OR RIPPLE BLANKING OUTPUT) PIN, A RIPPLE BLANKING INPUT PIN, AND A LAMP TEST FEATURE FOR ALL SEGMENTS. OPEN COLLECTOR OUTPUTS ARE PROVIDED WITH 40 MA DRIVE CAPABILITY AND A MAX OUTPUT VOLTAGE OF 15V.

KEY TO LOGIC SYMBOLS

CODE IDENT
DATA BASE REV 0

DWG NO 95387500

REV H

SHEET 148

TRUTH TABLE (PIN NO.)
POS LOGIC

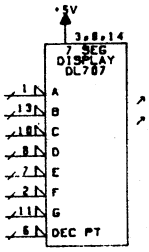
DECIMAL OR FUNCTION	INPUTS						BI/RBO (4)	OUTPUTS							NOTES
	LT(3)	RBI (5)	B(6)	4(2)	2(1)	1(7)		A(13)	B(12)	C(11)	D(10)	E(9)	F(15)	G(14)	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H= HI LOGIC LEVEL L= LOW LOGIC LEVEL X= IRRELEVANT

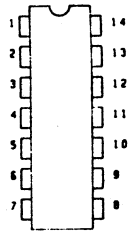
NOTES:
1. THE BLANKING INPUT (BI/RBO) MUST BE OPEN OR HELD AT A HIGH LOGIC LEVEL WHEN OUTPUT FUNCTIONS 0 TO 15 ARE DESIRED. THE RIPPLE BLANKING INPUT (RBI) MUST BE OPEN OR HIGH IF BLANKING OF A DECIMAL ZERO IS NOT DESIRED.
2. LOW LEVEL APPLIED TO (BI/RBO) , ALL SEGMENTS ARE OFF AND ALL OTHER INPUTS ARE (DON'T CARES).
3. WITH RBI AND INPUTS 8,4,2, AND 1 ARE LOW AND LAMPTEST IS HIGH, ALL SEGMENTS ARE OFF, AND THE BI/RBO GOES LOW AS A RESPONSE.
4. WITH BI/RBO IS OPEN OR HIGH AND A LOW IS APPLIED TO LAMPTEST, ALL SEGMENTS GO ON.

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #7447A

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A RED NUMERIC LED DISPLAY. IT PROVIDES .3 INCH HIGH CHARACTERS WITH WIDE ANGLE VIEWING CAPABILITY. A LEFT HAND DECIMAL POINT IS PROVIDED.

TRUTH TABLE (PIN NO.)
POS LOGIC

INPUT								DECIMAL DISPLAY OUTPUT FUNCTION
A (1)	B (13)	C (10)	D (8)	E (7)	F (2)	G (11)	DEC PT (6)	
L	L	L	L	L	L	H	H	0
H	L	L	H	H	H	H	H	1
L	L	H	L	L	H	L	H	2
L	L	L	L	H	H	L	H	3
H	L	L	H	H	L	L	H	4
L	H	L	L	H	L	L	H	5
H	H	L	L	L	L	L	H	6
L	L	L	H	H	H	H	H	7
L	L	L	L	L	L	L	H	8
L	L	L	H	H	L	L	H	9
H	H	H	L	L	H	L	H	NON FUNCTIONAL
H	H	L	L	H	H	L	H	NON FUNCTIONAL
H	L	H	H	H	L	L	H	NON FUNCTIONAL
L	H	H	L	H	L	L	H	NON FUNCTIONAL
H	H	H	L	L	L	L	H	NON FUNCTIONAL
H	H	H	H	H	H	H	H	BLANK
X	X	X	X	X	X	X	L	DECIMAL PT.

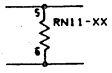
H= OPEN OR DRIVE CIRCUIT OFF
L= LOW OR DRIVE CIRCUIT ON
X= IRRELEVANT

ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION #DL707

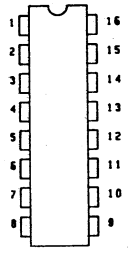
KEY TO LOGIC SYMBOLS

CODE IDENT DATA BASE REV G | C | DWG NO 95387500 | REV G | SHEET 149

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	G
DWG NO	95387500
CODE IDENT	C
SHEET 1 SD	

KEY TO LOGIC SYMBOLS

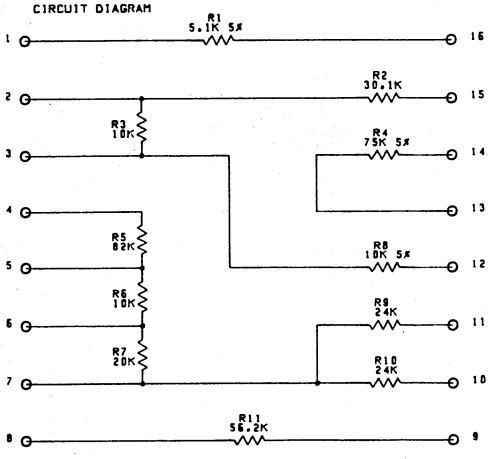
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS AN IN-LINE RESISTOR NETWORK.

CIRCUIT DIAGRAM

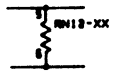


ELEMENT IDENTIFICATION #

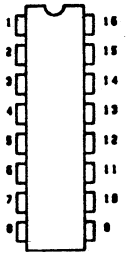
VENDOR IDENTIFICATION # 44672788

NETWORK IDENTIFICATION # RN11

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	G
DWG NO	95387500
CODE IDENT	C
SHEET 151	

KEY TO LOGIC SYMBOLS

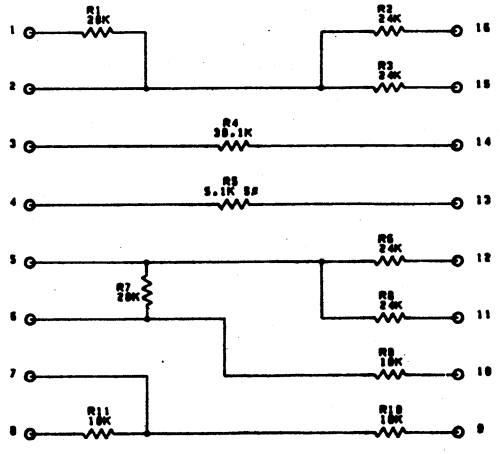
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS AN IN-LINE RESISTOR NETWORK.

CIRCUIT DIAGRAM

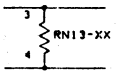


ELEMENT IDENTIFICATION 8

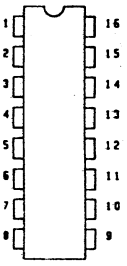
VENDOR IDENTIFICATION 8 44672787

NETWORK IDENTIFICATION 8 RN12

SYMBOLS/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV G

DWG NO 95387500

SHEET 1 S2

CODE IDENT C

KEY TO LOGIC SYMBOLS

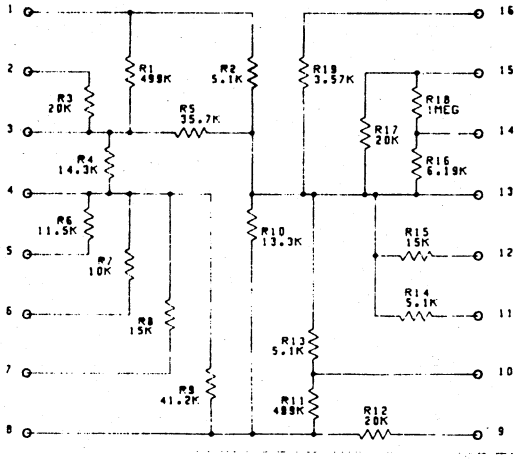
TRUTH TABLE

N/A

GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE IS A DUAL-IN-LINE RESISTOR NETWORK.

CIRCUIT DIAGRAM

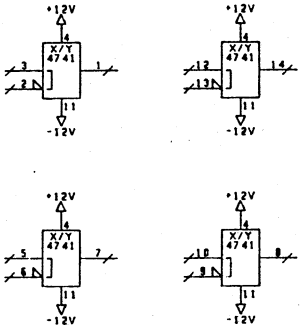


ELEMENT IDENTIFICATION #

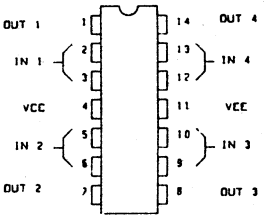
VENDOR IDENTIFICATION # 44672529

NETWORK IDENTIFICATION # RN13

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



REV	G
DWG NO	95387500
SHEET 1	1
CODE IDENT	C

KEY TO LOGIC SYMBOLS

TRUTH TABLE

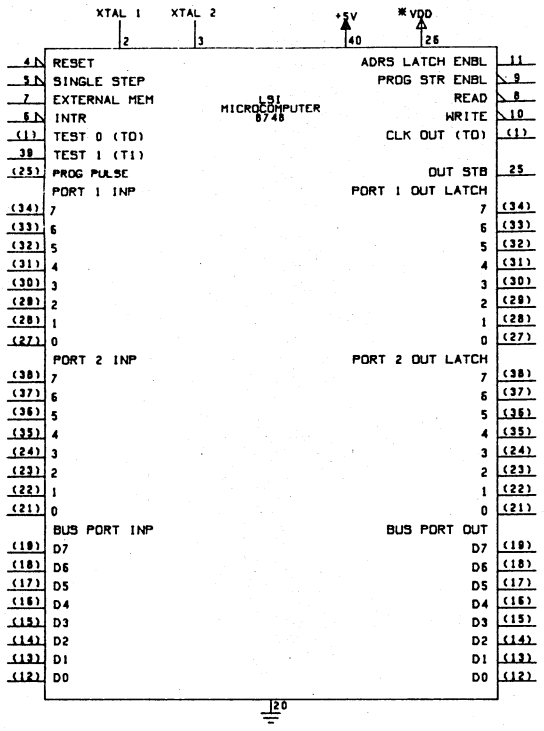
GENERAL OPERATIONAL DESCRIPTION

THE 4741 SERIES IS A TRUE QUAD 741. IT CONSISTS OF FOUR INDEPENDENT, HIGH GAIN, INTERNALLY COMPENSATED, LOW POWER OPERATIONAL AMPLIFIERS WHICH HAVE BEEN DESIGNED TO PROVIDE FUNCTIONAL CHARACTERISTICS IDENTICAL TO THOSE OF THE FAMILIAR 741 OPERATIONAL AMPLIFIER. IN ADDITION THE TOTAL SUPPLY CURRENT FOR ALL FOUR AMPLIFIERS IS COMPARABLE TO THE SUPPLY CURRENT OF A SINGLE 741 TYPE OP AMP. OTHER FEATURES INCLUDE INPUT OFFSET CURRENTS AND INPUT BIAS CURRENT WHICH ARE MUCH LESS THAN THOSE OF A STANDARD 741. ALSO, EXCELLENT ISOLATION BETWEEN AMPLIFIERS HAS BEEN ACHIEVED BY INDEPENDENTLY BIASING EACH AMPLIFIER AND USING LAYOUT TECHNIQUES WHICH MINIMIZE THERMAL COUPLING.

TIMING DIAGRAM

ELEMENT IDENTIFICATION #
VERDOR IDENTIFICATION # LM348/4741

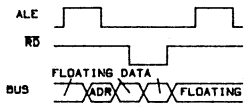
SYMBOL/APPLICATION/PINS



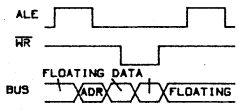
*VDD =+25V DURING PROGRAMMING
=+5V DURING OPERATION

TIMING DIAGRAMS

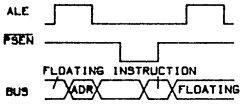
READ FROM EXTERNAL MEMORY



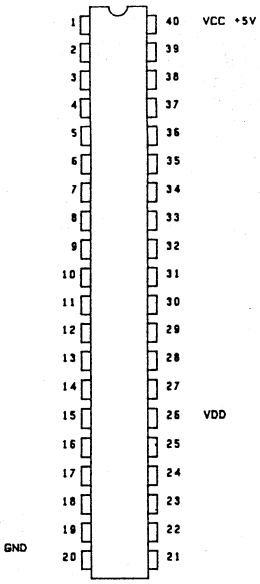
WRITE TO EXTERNAL MEMORY



INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



MECHANICAL CONFIGURATION
(TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THE 8748 IS AN 8-BIT PARALLEL COMPUTER. IT CONTAINS A 1KX8 EPROM, 64X8 RAM, 27 I/O LINES, AND AN 8-BIT TIMER/ CONTER. THREE OF THE PROGRAM RESIDENT MEMORIES ARE OF SPECIAL IMPORTANCE. LOCATIONS 0,3 AND 7. THE RESIDENT RAM MEMORY HAS TWO 8 WORKING REGISTER BANKS AND 8 LEVEL STACK. THE 27 I/O LINES ARE GROUPED AS 3 TEST PINS AND 3 PORTS.

PORT 1 = 8-BIT QUASI-BIDIRECTIONAL PORT. OUTPUTS ARE LATCHED BUT INPUTS ARE NOT LATCHED.

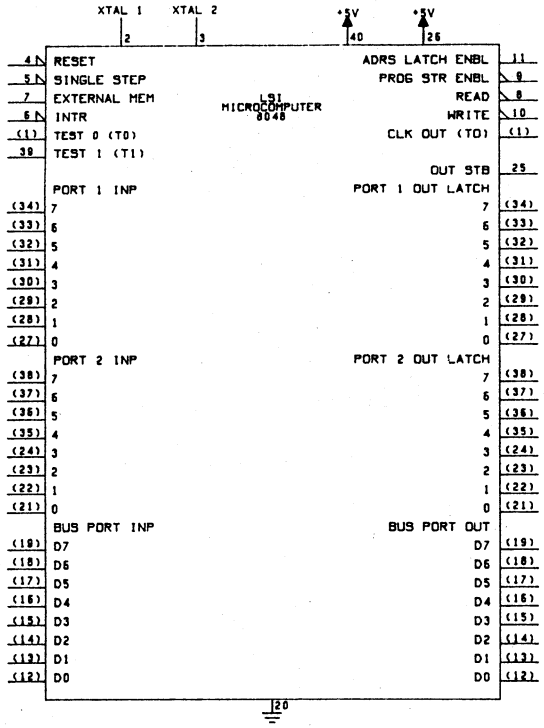
PORT 2 = 8-BIT QUASI-BIDIRECTIONAL PORT. OUTPUTS ARE LATCHED BUT INPUTS ARE NOT LATCHED. THE LOW ORDER 4-BITS CONTAIN THE 4 HIGH ORDER PROGRAM COUNTER BITS FOR EXTERNAL PROGRAM MEMORY FETCH AND SERVE AS 4-BIT I/O EXPANDER BUS FOR 8243.

BUS = 8-BIT BIDIRECTIONAL PORT. CONTAINS THE 8 LOW ORDER PROGRAM COUNTER BITS AND DATA FOR EXTERNAL PROGRAM MEMORY. ALSO CONTAINS THE ADDRESS AND DATA FOR EXTERNAL RAM MEMORY.

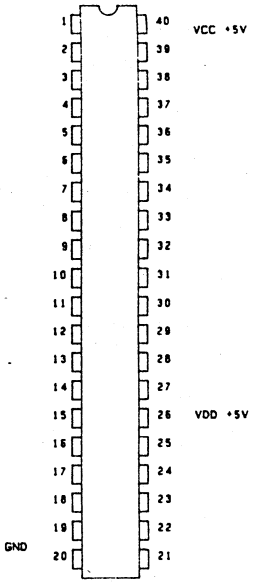
ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 8748

SYMBOL/APPLICATION/PINS

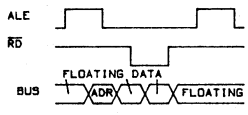


MECHANICAL CONFIGURATION
(TOP VIEW)

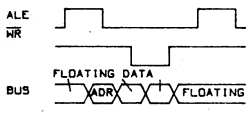


TIMING DIAGRAMS

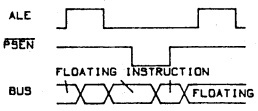
READ FROM EXTERNAL MEMORY



WRITE TO EXTERNAL MEMORY



INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



GENERAL OPERATIONAL DESCRIPTION

THE 8048 IS AN 8-BIT PARALLEL COMPUTER. IT CONTAINS A 1KX8 ROM, 64X8 RAM, 27 I/O LINES, AND AN 8-BIT TIMER/COUNTER. THREE OF THE PROGRAM RESIDENT MEMORIES ARE OF SPECIAL IMPORTANCE, LOCATIONS 0, 3 AND 7. THE RESIDENT RAM MEMORY HAS TWO 8 WORKING REGISTER BANKS AND 8 LEVEL STACK. THE 27 I/O LINES ARE GROUNDED AS 3-TEST PINS AND 3 PORTS.

PORT 1 = 8-BIT QUASI-BIDIRECTIONAL PORT. OUTPUTS ARE LATCHED BUT INPUTS ARE NOT LATCHED.

PORT 2 = 8-BIT QUASI-BIDIRECTIONAL PORT. OUTPUTS ARE LATCHED BUT INPUTS ARE NOT LATCHED. THE LOW ORDER 4-BIT CONTAIN THE 4 HIGH ORDER PROGRAM COUNTER BITS FOR EXTERNAL PROGRAM MEMORY FETCH AND SERVE AS 4-BIT I/O EXPANDER BUS FOR 8243.

BUS = 8-BIT BIDIRECTIONAL PORT. CONTAINS THE 8 LOW ORDER PROGRAM COUNTER BITS AND DATA FOR EXTERNAL PROGRAM MEMORY. ALSO CONTAINS THE ADDRESS AND DATA FOR EXTERNAL RAM MEMORY.

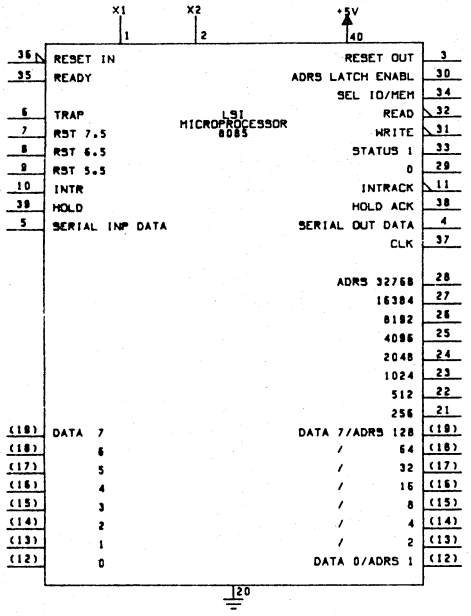
ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 8048

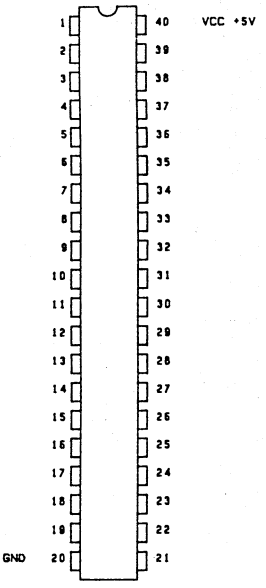
KEY TO LOGIC SYMBOLS

CODE IDENT C DWG NO 95387500 REV 1 SHEET 155

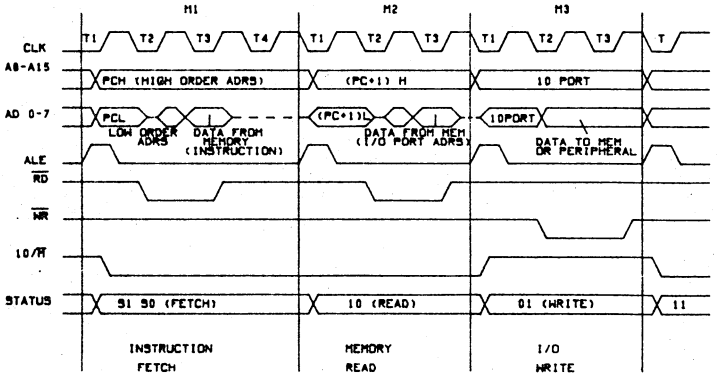
SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION
(TOP VIEW)



TIMING DIAGRAM
BASIC SYSTEM TIMING



GENERAL OPERATIONAL DESCRIPTION

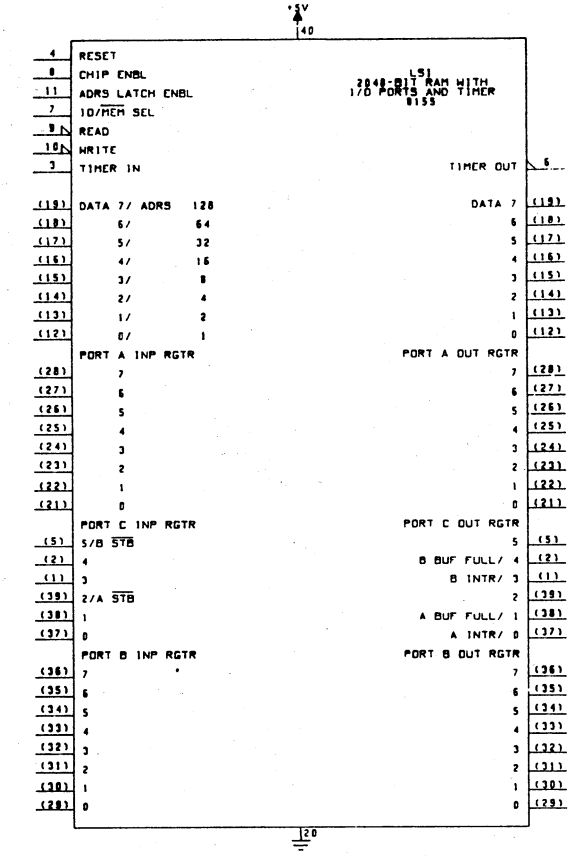
THE 8085 IS A COMPLETE 8-BIT PARALLEL CENTRAL PROCESSING UNIT. IT IMPROVES THE 8080'S PERFORMANCE BY HIGHER SYSTEM SPEED AND IT INCORPORATES ALL OF THE FEATURES THAT THE 8224 AND 8228 PROVIDE FOR 8080. THE 8085 USES A MULTIPLEXED DATA BUS. PLUS THE 8080 INTR INPUT, IT HAS THREE MASKABLE RESTART INTERRUPTS AND ONE NON MASKABLE INTERRUPT. IT ALSO PROVIDES SERIAL INPUT DATA AND SERIAL OUTPUT DATA LINES FOR SIMPLE SERIAL INTERFACE.

ELEMENT IDENTIFICATION #

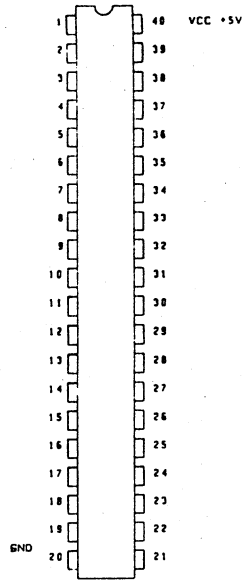
VENDOR IDENTIFICATION # 8085

REV I
DWG NO 95387500
SHEET 156
CODE IDENT C
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



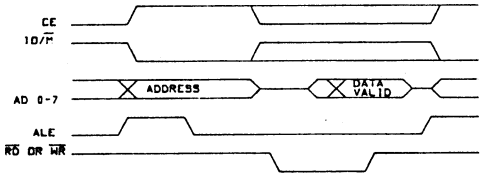
MECHANICAL CONFIGURATION
(TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

~~THE 8155~~ CONSISTS OF 256X8 STATIC RAM, I/O PORTS AND A TIMER. THE I/O PORTION CONSISTS OF TWO 8-BIT PORTS WHICH CAN BE PROGRAMMED FOR EITHER INPUT OR OUTPUT. THE THIRD IS A 6-BIT PORT WHICH CAN BE PROGRAMMED AS AN INPUT, AS AN OUTPUT, OR AS STATUS TO ALLOW THE OTHER TWO PORTS TO OPERATE IN HANDSHAKE MODE. THE 14-BIT PROGRAMMABLE COUNTER/TIMER CAN PROVIDE A SQUARE WAVE OR TERMINAL COUNT PULSE.

TIMING DIAGRAM

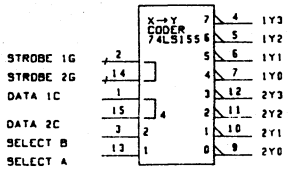


ELEMENT IDENTIFICATION #

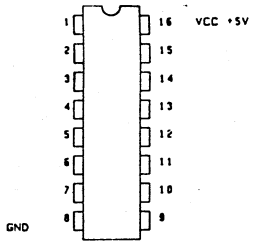
VENDOR IDENTIFICATION # 8155

REV H
DWG NO 95387500
SIZE C
SHEET 157
CODE IDENT
KEY TO LOGIC SYMBOLS

SYMBOLS/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	G	C	Y0	Y1	Y2	Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

X = IRREVELENT

GENERAL OPERATIONAL DESCRIPTION

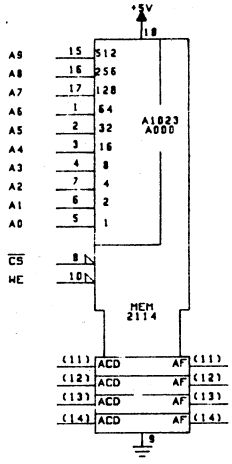
THIS DUAL 1-LINE TO 4-LINE DEMULTIPLEXER HAS INDIVIDUAL STROBES AND COMMON BINARY-ADDRESS INPUTS. WHEN BOTH SECTIONS ARE ENABLED THE STROBES, THE COMMON BINARY ADDRESS INPUTS SEQUENTIALLY SELECT AND ROUTE ASSOCIATED INPUT DATA TO THE APPROPIATE OUTPUT OF EACH SECTION. THE INDIVIDUAL STROBES PERMIT ACTIVATING OR INHIBITING EACH OF THE 4-BIT SECTION AS DESIRED. DATA APPLIED TO INPUT 1C IS INVERTED AT ITS OUTPUTS AND DATA APPLIED AT 2C IS NOT INVERTED THROUGH ITS OUTPUTS. THE INVERTER FOLLOWING THE IC DATA INPUT PERMITS USE AS A 3-TO-8 LINE DECODER OR 1-TO-8 LINE DEMULTIPLEXER WITHOUT EXTERNAL GATING. INPUT CLAMPING DIODES ARE PROVIDED ON ALL OF THESE CIRCUITS TO MINIMIZE TRANSMISSION-LINE EFFECTS AND SIMPLIFY SYSTEM DESIGN.

TIMING DIAGRAM.

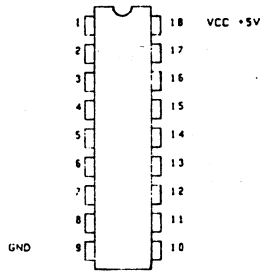
ELEMENT IDENTIFICATION #
VENDOR IDENTIFICATION # 74LS155

REV H
DWG NO 95387500
CODE IDENT C
SHEET 158
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS

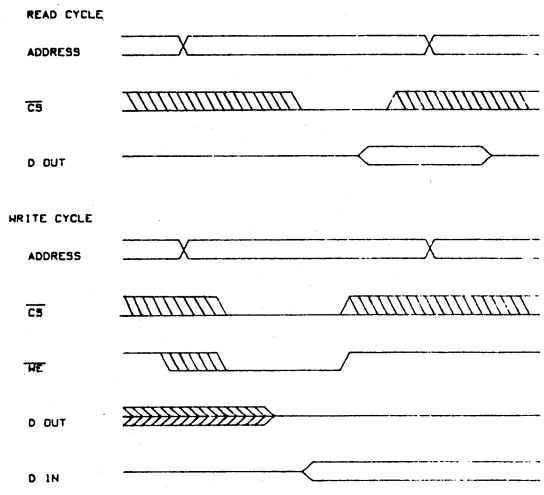


MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE
POS LOGIC

TIMING DIAGRAMS



GENERAL OPERATIONAL DESCRIPTION

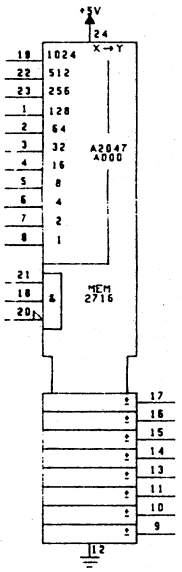
THE 2114 IS A 4096 BIT STATIC RANDOM ACCESS MEMORY ORGANIZED AS 1024 WORDS BY 4 BITS. IT IS DIRECTLY TTL COMPATIBLE IN ALL RESPECTS ; INPUTS, OUTPUTS, AND A SINGLE +5V SUPPLY. A SEPRATE CHIP SELECT ($\overline{CS}$) LEAD ALLOWS THE SELECTIONS OF INDIVIDUAL CHIP WHEN OUTPUTS ARE OR TIED.

ELEMENT IDENTIFICATION #

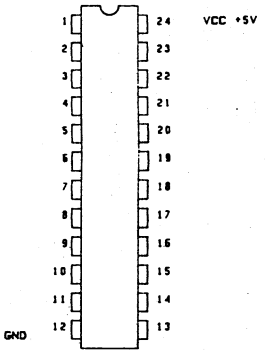
VENDOR IDENTIFICATION # 2114

REV H
DWG NO 95387500
C
SHEET 158
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS

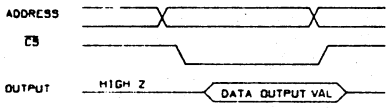


MECHANICAL CONFIGURATION
(TOP VIEW)

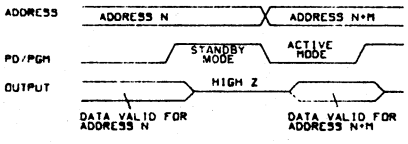


TIMING DIAGRAMS

READ MODE PD/PGM = VIL



SATNDBY MODE $\overline{CS}$ = VIL



GENERAL OPERATIONAL DESCRIPTION

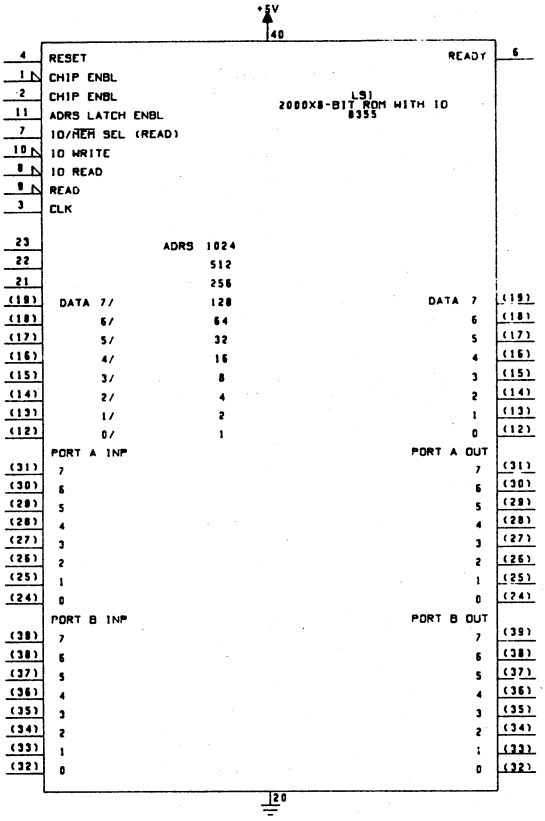
THE 2716 IS A 16,384-BIT ERASABLE AND ELLELTRICALLY PROGRAMMABLE READ ONLY MEMORY. ORGANIZED AS 2048 WORDS BY 8-BITS. IT IS THE FIRST EPROM WITH A STATIC POWER DOWN MODE. THE RECOMMENDED ERASURE PROCEDURE IS EXPOSURE TO SHORTHAVE ULTRAVIOLET LIGHT.

ELEMENT IDENTIFICATION #

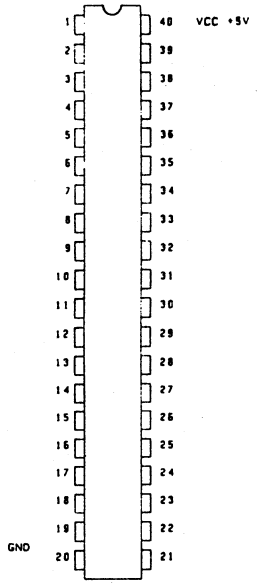
VENDOR IDENTIFICATION # 2716

REV H
C 95387500
DWG NO
SHEET 160
CODE IDENT
KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



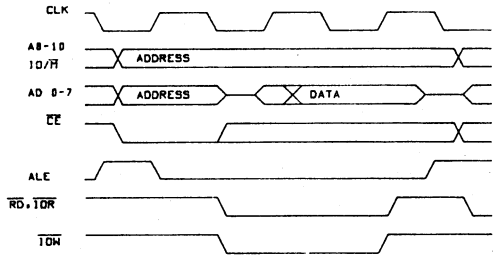
MECHANICAL CONFIGURATION
(TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THE 8355 IS A ROM AND I/O CHIP. THE ROM PORTION IS ORGANIZED AS 2048 WORDS X 8 BIT. THE I/O PORTION CONSISTS OF TWO GENERAL PURPOSE I/O PORTS. EACH I/O PORT HAS 8 PORT LINES. AND EACH I/O PORT LINE IS INDIVIDUALLY PROGRAMMABLE AS INPUT OR OUTPUT.

TIMING DIAGRAM
ROM READ AND I/O READ AND WRITE



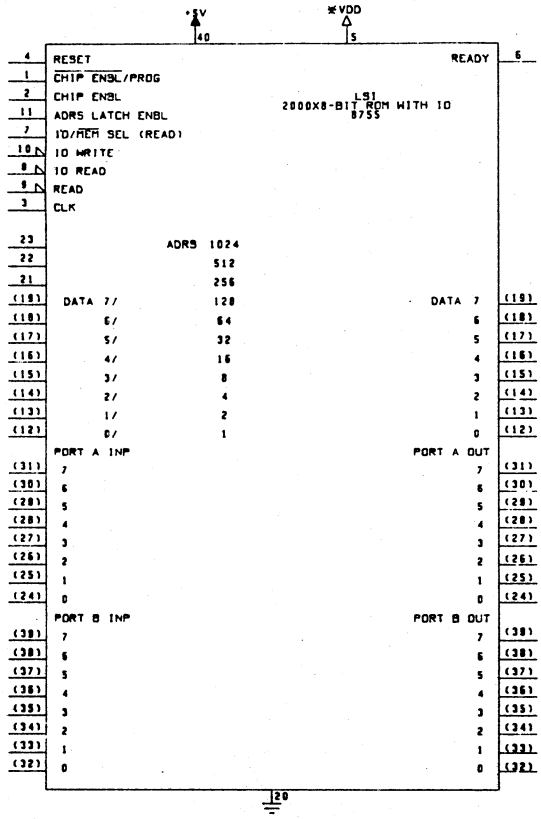
ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 8355

KEY TO LOGIC SYMBOLS

DWG NO 95387500 REV H
SIZE C
SHEET 161

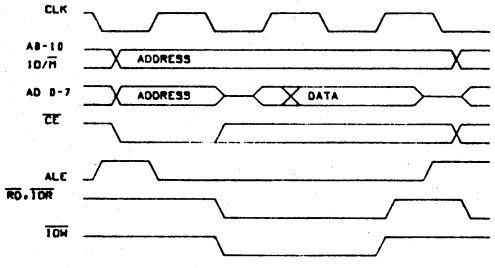
SYMBOL/APPLICATION/PINS



* VDD AND $\overline{CE}$/PROG PINS HAVE SPECIAL FUNCTIONS IN THE PROGRAMMING PROCUDURE. IN OPERATION VDD IS GROUNDED.

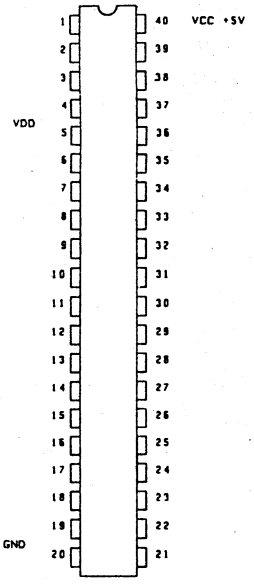
TIMING DIAGRAM

PROM READ AND I/O WRITE TIMING



MECHANICAL CONFIGURATION

(TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THE 8755 IS AN EPROM AND I/O CHIP. THE EPROM PORTION IS ORGANIZED AS 2048 WORDS X 8 BITS. THE I/O PORTION CONSISTS OF TWO GENERAL PURPOSE I/O PORTS. EACH I/O PORT HAS 8 PORT LINES, AND EACH I/O PORT LINE IS INDIVIDUALLY PROGRAMMABLE AS INPUT OR OUTPUT.

ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 8755

REV H

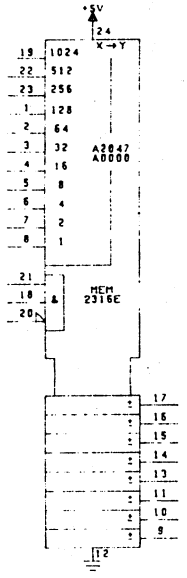
DWG NO C 95387500

SHEET 182

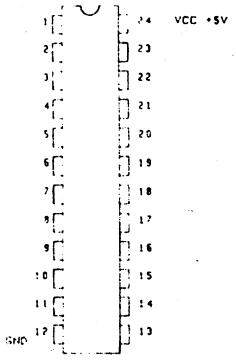
CODE IDENT

KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS



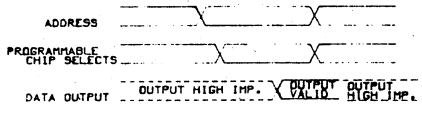
MECHANICAL CONFIGURATION
(TOP VIEW)



REV H
DWG NO 95387500
C
CODE IDENT
SHEET 163

KEY TO LOGIC SYMBOLS

TIMING DIAGRAM



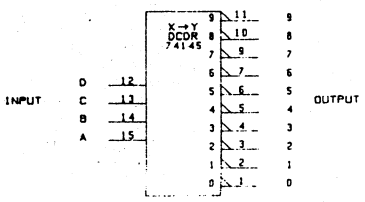
GENERAL OPERATIONAL DESCRIPTION

THE 2316E IS A 16,384-BIT STATIC N-CHANNEL MOS READ ONLY MEMORY ORGANIZED AS 2048 WORDS BY 8 BITS THE CIRCUIT FEATURES THREE PROGRAMMABLE CHIP SELECTS WHICH MAY BE DEFINED BY THE USER AND ARE FIXED DURING THE MASKING PROCESS.

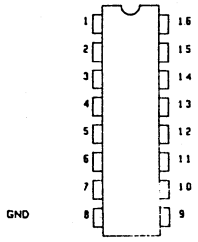
ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 2316E

SYMBOL/APPLICATION/PINS



MECHANICAL CONFIGURATION (TOP VIEW)



TRUTH TABLE

POS LOGIC

BCD INPUTS				DECIMAL OUTPUT									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

GENERAL OPERATIONAL DESCRIPTION

THIS MONOLITHIC DECIMAL DECODER CONSISTS OF EIGHT INVERTERS AND TEN FOUR-INPUT NAND GATES. THE INVERTERS ARE CONNECTED IN PAIRS TO MAKE BCD INPUT DATA AVAILABLE FOR DECODING BY THE NAND GATES. FULL DECODING OF VALID INPUT LOGIC ENSURES THAT ALL OUTPUTS REMAIN OFF FOR ALL INVALID INPUT CONDITIONS.

ELEMENT IDENTIFICATION

VENDOR IDENTIFICATION 74145

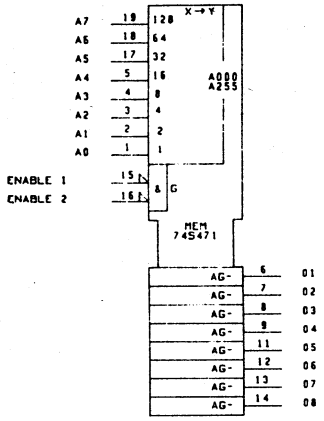
REV H

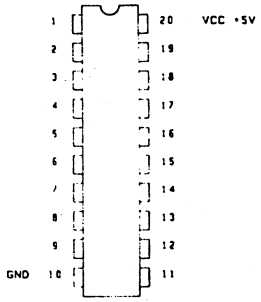
DWG NO C 95387500

SHEET 184

KEY TO LOGIC SYMBOLS

SYMBOL/APPLICATION/PINS





ELEMENT IDENTIFICATION #

VENDOR IDENTIFICATION # 745471

REV H

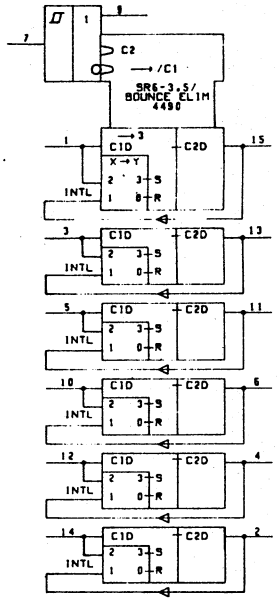
DWG NO 95387500

SHEET 165

CODE IDENT C

KEY TO LOGIC SYMBOLS

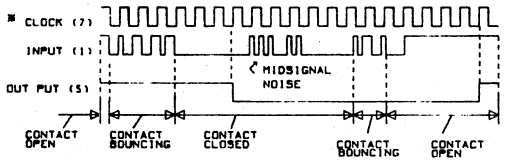
SYMBOL AND LEVELS



VCC = PIN 16=+5V
VSS = PIN 8=GND

	NOM	MIN	MAX	UNIT
HI INPUT VOLTAGE	+3.3	---	VCC+0.5	V
LO INPUT VOLTAGE	+0.2	---	VSS-0.5	V
HI INPUT VOLTAGE	+3.3	+2.4	---	V
LO INPUT VOLTAGE	+0.2	---	+0.4	V
VCC	+5.0	-0.5	+6.0	V

WAVEFORMS

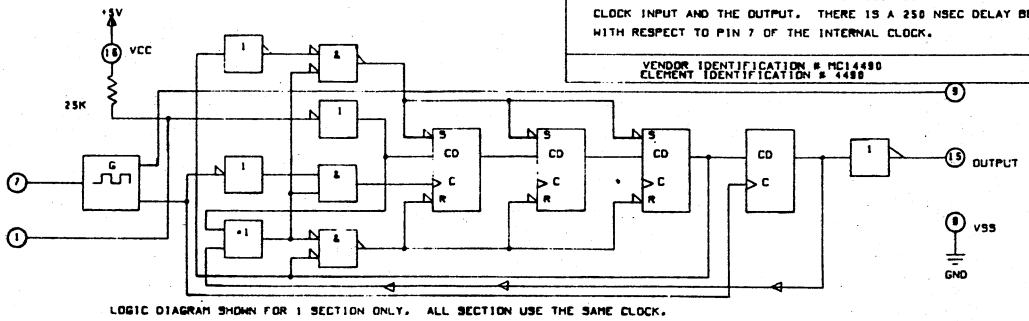


WHEN A CAPACITOR IS NOT CONNECTED ACROSS PINS 7 & 8, PIN 8 IS A BUFFERED OUTPUT OF THE SIGNAL APPLIED TO PIN 7

WAVEFORMS SHOWN FOR ONE CONTACT BOUNCE ELIMINATOR ONLY.

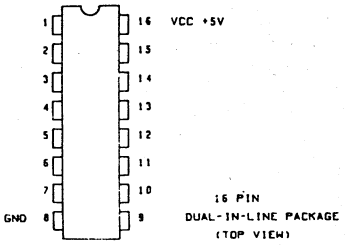
THE OUTPUT WILL BE THE SAME AS THE CLEAN INPUT SIGNAL +1 CLOCK PERIOD

LOGIC DIAGRAM



LOGIC DIAGRAM SHOWN FOR 1 SECTION ONLY. ALL SECTION USE THE SAME CLOCK.

MECHANICAL CONFIGURATION (TOP VIEW)



16 PIN
DUAL-IN-LINE PACKAGE
(TOP VIEW)

OPERATIONAL DESCRIPTION

THE TYPE 4490 IS A HEX CONTACT BOUNCE ELIMANATOR USED TO ELIMINATE EXTRANEOUS SIGNALS (BOUNCE) ON BOTH THE LEADING AND TRAILING EDGES OF A SIGNAL. RESULTING FROM SWITCH OPERATION. EACH ELIMINATOR CONSISTS OF A 3 1/2 BIT SHAFT REGISTER (SR) AND LOGIC TO COMPARE THE INPUT WITH THE CONTENTS OF THE SR. AN EXTERNAL CLOCK MAY BE CONNECTED TO PIN 7 OR A SMALL CAPACITOR MAY BE CONNECTED ACROSS PIN 7 AND PIN 8 TO START THE INTERNAL CLOCK. THE LOW GOING EDGE OF THE CLOCK SHIFTS THE INPUT LEVEL INTO EACH SR LOCATION. A CLEAN DIGITAL SIGNAL GENERATED 3 1/2 TO 4 1/2 CLOCK PERIODS AFTER THE INPUT HAS STABILIZED. EACH OUTPUT IS CAPABLE OF DRIVING 2 TTL LOADS AND AN INTERNAL PULL UP RESISTOR (APPROX. 25K) IS USED ON EACH DATA INPUT.

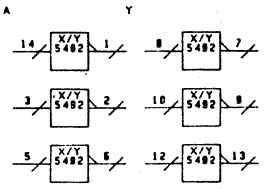
ASSUME ALL BITS OF THE SR (3 1/2 BITS) ARE LO. THE OUTPUT IS HI AND THE INPUT IS HI (CONTACT OPEN). WHEN THE INPUT GOES LO (CONTACT CLOSED), A HI IS ENTERED INTO THE SR (1 BIT) ON THE LO GOING CLOCK. FOLLOWING THIS AN OPEN CONTACT WITHIN 3 1/2 CLOCK PERIODS. CAUSES THE LOGIC TO DIRECTLY RESET THE SR LO (3 BITS) AND THE TIMING SEQUENCE STARTS ALL OVER AGAIN WHEN THE CONTACT RE-CLOSES. EVENTUALLY THE LO INPUT STABILIZES AND A HI IS SHIFTED THROUGH THE SR (3 1/2 BITS). IN CONJUNCTION WITH THE CLOCK INPUT TRANSITION. NOTE THAT DATA ENTERS THE LAST STAGE OF THE SR ON THE POSITIVE GOING EDGE OF THE CLOCK. ACCOUNTING FOR THE 1/2 BIT. THIS RESULTS IN A LO OUTPUT 3 1/2 - 4 1/2 CLOCK PERIODS AFTER THE CONTACT HAS CLOSED (STABLE LO INPUT). MIDSIGNAL NOISE, OF ANY LENGTH (ASSUMING NO STABLE PERIOD LONGER THAN 3 1/2 CLOCK PERIODS) HAS NO EFFECT ON THE OUTPUT.

ASSUME THAT WITH THE CONTACT CLOSED AND THE OUTPUT LO, THAT THE CONTACT NOW OPENS. THIS FURNISHES A HI INPUT AND A LO ENTERS THE SR (1 BIT). FOLLOWING THIS THE CONTACT BOUNCES CLOSED PROVIDING A LO INPUT AND CAUSING THE LOGIC TO DIRECTLY SET THE SR HI (3 BITS). AS BEFORE THE TIMING SEQUENCE STARTS OVER WHEN THE CONTACT RE-OPENS. WHEN THE INPUT STABILIZES TO A HI LEVEL, A LO IS SHIFTED THROUGH THE SR (3 1/2) BITS AND THE OUTPUT GOES HI 3 1/2 TO 4 1/2 CLOCK PERIODS AFTER THE CONTACT HAS OPENED. THE INTERNAL OSCILLATOR FREQUENCY MAY BE CALCULATED FROM THE FORMULA $F=\frac{0.375}{CEXT}$ VCC, WHERE CEXT IS IN PF AND F IS IN MHZ. A DELAY OF APPROXIMATELY 488 NSEC OCCURS BETWEEN THE HI GOING CLOCK INPUT AND THE OUTPUT. THERE IS A 250 NSEC DELAY BETWEEN PIN 8 WITH RESPECT TO PIN 7 OF THE INTERNAL CLOCK.

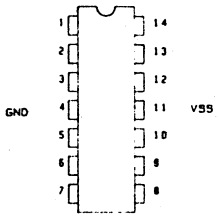
VENDOR IDENTIFICATION # MC14490
CLEMENT IDENTIFICATION # 4490

REV H
DWG NO C 95387500
SHEET 186
CODE IDENT
KEY TO LOGIC SYMBOLS

LOGIC SYMBOL

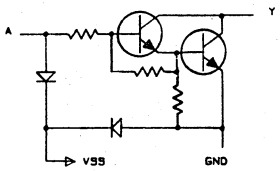


MECHANICAL PACKAGE
(TOP VIEW)



SCHEMATIC

(ONE OF SIX)



GENERAL DESCRIPTION

THIS DEVICE IS INTENDED FOR USE AS AN INTERFACE CIRCUIT IN CONJUNCTION WITH MOS INTERGRATED CIRCUIT AND COMMON-CATHODE LED'S IN SERIALLY ADDRESSED MULTI-DIGIT DISPLAYS.

EACH INVERTER SECTION IS CAPEABLE OF SINKING A MAXIMUM OF 250 MA CURRENT WITH A LOW CURRENT DRIVE INPUT INTERFACING WITH MOS DEVICES

THE MAXIMUM AVERAGE CURRENT SINKING CAPABILITY FOR THE ENTIRE PACKAGE IS 600 MA.

THE MAXIMUM OPERATING VOLTAGE VSS IS 10VDC.

TRUTH TABLE

POS LOGIC

$Y = \overline{A}$

A	Y
1	0
0	1

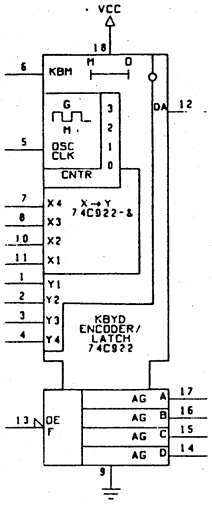
ELEMENT IDENTIFICATION # 5482

VENDOR IDENTIFICATION # DS75482

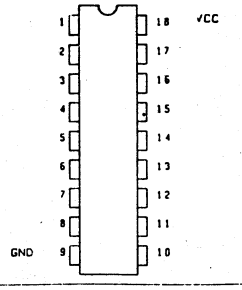
REV H
DWG NO 95387500
SIZE C
SHEET 187
KCOR FORMAT

KEY TO LOGIC SYMBOLS

LOGIC SYMBOL



MECHANICAL OUTLINE
(TOP VIEW)



TRUTH TABLE

SWITCH CONTACT		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4
DATA OUT	A	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1
	D	0	0	0	0	0	0	0	0

SWITCH CONTACT		8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4
DATA OUT	A	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1
	D	1	1	1	1	1	1	1	1

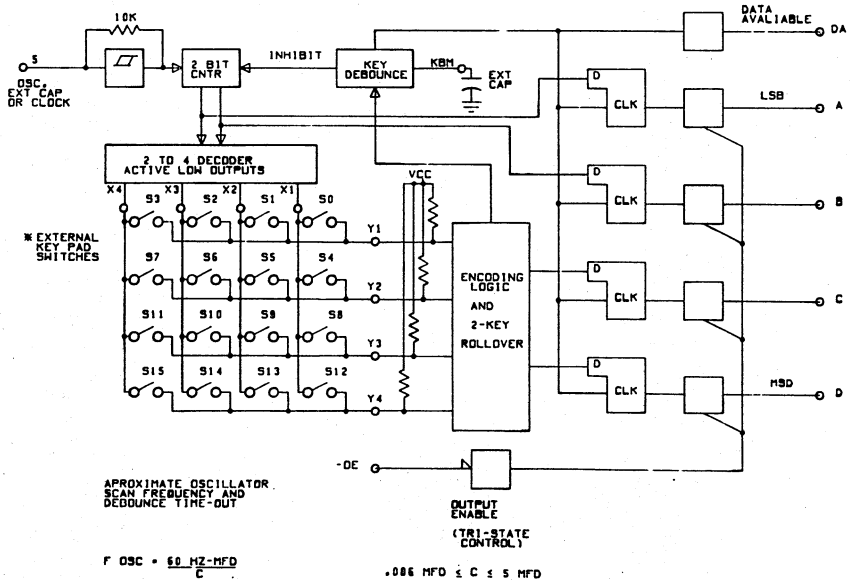
GENERAL DESCRIPTION

THIS CMOS KEY ENCODER PROVIDES ALL NECESSARY LOGIC TO FULLY DECODE AN ARRAY OF SIXTEEN SPST SWITCHES. THE KEYBOARD SCAN CAN BE IMPLEMENTED BY USING AN EXTERNAL CLOCK OR AN EXTERNAL CAPACITOR WHICH CAUSES THE INTERNAL LOGIC TO OSCILLATE AT A SPECIFIC SELECTED FREQUENCY. THE OUTPUT ENCODED SWITCH CLOSURE DATA IS STROBED INTO TRI-STATE LATCHES AFTER A FIXED DEBOUNCE DELAY SELECTED BY AN EXTERNAL CAPACITOR. THIS DELAYED STROBE ALSO FUNCTIONS AS A DATA AVAILABLE LOGIC SIGNAL INDICATING THAT THE DATA STORED IN THE LATCHES IS VALID. THE OUTPUT ENABLE NOT LINE ACTIVATES THE TRI-STATE OUTPUTS. TO A TTL COMPATIBLE LOGIC "0" OR "1" STATE. THE OUTPUTS ARE NORMALLY IN AN INACTIVE HIGH IMPEDANCE STATE.

FOLLOWING THE BLOCK DIAGRAM, OPERATION IS AS FOLLOWING: THE INTERNAL 2 BIT COUNTER DRIVEN BY THE INTERNAL OSCILLATOR OR EXTERNAL CLOCK SEQUENTIALLY SCANS THE X SWITCH LINES WITH AN ACTIVE LOW SIGNAL. IF A SWITCH IS CLOSED, THIS LOW SIGNAL IS APPLIED TO ONE OF THE Y SWITCH LINES THRU THE CLOSED SWITCH. THE INTERNAL LOGIC SENSES THAT A Y LINE WAS ACTIVATED, ENCODES THE INFORMATION AND APPLIES THE DATA TO THE LATCHES. AT THE SAME TIME, A DELAY TIMER IS ACTIVATED. AT THE END OF THIS DELAY PERIOD SELECTED BY AN EXTERNAL CAPACITOR C (KBM), THE ENCODED SWITCH CLOSURE DATA IS LATCHED AND THE DATA AVALIABLE LINE GOES "HIGH" INDICATING STABLE VALID DATA FOR THE DURATION OF SWITCH CLOSURE. THE OUTPUT ENABLE NOT LINE CAN THEN BE ACTIVATED TO READ THE OUTPUT DATA LINES.

A TWO KEY ROLL-OVER FUNCTION IS PROVIDED. THE FIRST SWITCH DEPRESSED OF TWO SIMULTANEOUS CLOSURES WILL BE VALIDATED. THE SECOND SWITCH WILL BE IGNORED UNTIL THE FIRST SWITCH IS RELEASED.

BLOCK DIAGRAM



APROXIMATE OSCILLATOR SCAN FREQUENCY AND DEBOUNCE TIME-OUT

$F_{OSC} = \frac{60\ HZ\text{-}MFD}{C}$

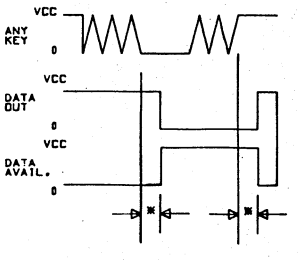
KBM = 10 MILISEC/MFD

.006 MFD ≤ C ≤ 5 MFD

.1 MFD ≤ C ≤ 100 MFD

ELEMENT I.D. # 74C922

VENDOR I.D. # MM74C922



* TDELAY DETERMINED BY C_{KBM}

REV H

DWG NO 95387500

SHEET 168

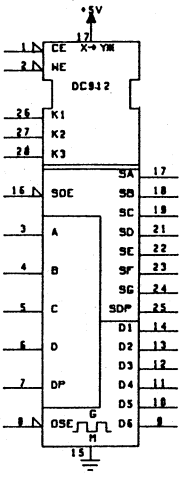
CODE IDENT C

KEY TO LOGIC SYMBOLS

REV	H
DWG NO	95387500
CODE IDENT	C
SHEET	1 OF 8

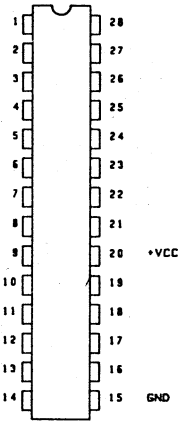
KEY TO LOGIC SYMBOLS

LOGIC SYMBOL



* THE ASTERISK INDICATES THE ITEM IS AN INCOMPLETE PORTRAYAL OF COMPLEX LOGIC

MECHANICAL PACKAGE (TOP VIEW)



GENERAL OPERATIONAL DESCRIPTION

THIS DEVICE, A DISPLAY CONTROLLER, SERVES AS AN INTERFACE DEVICE BETWEEN A DATA BUS AND A GROUP OF UP TO SIX OR SEVEN SEGMENT DIGITAL DISPLAYS. THE UNIT CONSIST OF STORAGE ELEMENTS TO STORE THE BINARY INFORMATION AND A DIGIT ADDRESS FOR EACH DATA BYTE TO BE DISPLAYED. A ROM ELEMENT DECODES THE STORED BINARY DATA INTO A SEVEN SEGMENT CODE TO OPERATE THE SEGMENT ELEMENTS OF THE DISPLAY.

AN INTERNAL OSCILLATOR SEQUENTIALLY SELECT A DIGIT AND THE SEGMENT INFORMATION FOR EACH DIGIT TO BE DISPLAYED. THUS A SIX DIGIT DISPLAY IS OPERATED IN A TIME MULTIPLEX MODE.

THE INPUT DATA MAY BE WRITTEN IN ANY DIGIT SEQUENCE INDEPENDENT OF THE DIGIT BEING DISPLAYED. THE INPUT DATA AND DIGIT ADDRESS MUST BE STABLE BEFORE THE WRITE ENABLE LINE (WE) IS ACTIVATED.

THE SEGMENT OUTPUT LINE CAN SOURCE 40MA OF CURRENT EACH. THE DIGIT SELECT LINES REQUIRE AN OUTPUT DRIVER TO SINK ALL THE SEVEN SEGMENT CURRENTS OF EACH DIGIT SINCE THE DEVICE CAN SOURCE ONLY 1MA OF CURRENT.
THE -SOE CONTROL ENABLES THE SEGMENT OUTPUTS WHEN LOW
THE -OSE CONTROL ENABLES THE OSSILLATOR TO RUN WHEN LOW
WHEN HIGH. A 1 APPLIED TO A DIGIT OUTPUT WILL SELECT THAT DIGIT'S SEGMENTS.

VENDOR IDENTIFICATION # MM74C912

ELEMENT IDENTIFICATION # DC912

BLOCK DIAGRAM